

A CURRENT-REGULATED VOLTAGE-CONTROLLED SCHEME
FOR DC TO AC VOLTAGE-SOURCE STATIC POWER SUPPLIES

CENTRE FOR NEWFOUNDLAND STUDIES

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A Current-Regulated Voltage-Controlled Scheme for DC to AC Voltage-Source Static Power Supplies

by

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Abstract

This thesis presents a cost-effective control strategy for fixed-switching frequency variable duty-cycle control of static voltage-source inverters with output filter for uninterruptible power supplies (UPS) and utility interactive systems (UIS). The proposed control scheme is based on sensing the current in the capacitor of the load filter and using it in an inner feedback loop. An outer capacitor voltage feedback loop is also incorporated to ensure well-regulated sinusoidal load voltage in UPS applications, and indirect regulation of the utility line current in UIS applications.

The performance of the proposed control scheme is examined for voltage-source inverters with output filter. A general model of the power circuit which includes the inverter and a second-order load filter, and the load is established for each application. These models are discontinuous because of the switching nature of the power inverter, but they are employed to obtain computer simulation results of various waveforms in the inverter system.

In order to examine the steady-state and dynamic behaviour of each system, analytical models are derived from the general model. Employing Fourier series analysis, a time-continuous model is derived from the system discontinuous model. For the three-phase systems, time-invariant models are obtained by transforming the time-continuous models to the rotating frame of reference using the forward-backward transformation for UPS and θ - q - d transformation for the UIS. Perturbation and small-signal approximations are applied to the time-invariant models to obtain steady-state and linearized small-signal models which are used to examine the steady-state and dynamic performance of the systems.

Using the root-locus analysis technique and pole-zero maps, the incremental dynamics of the power circuit state variables are investigated. In particular, the transfer functions of the incremental dynamics of the power circuit state variables due to incremental changes in the control signal are examined. The results of the investigation are used to select appropriate feedback variables in the control circuit such that a stable and successful operation of the feedback control scheme is achieved.

It is shown that choosing either the inverter output or capacitor current as the feedback variable in the system produces stable operation. Selection of the inverter output current as the feedback variable is overruled due to possible harmonic instability in the load circuit or the need for an extra load current sensor. Consequently, the capacitor current is chosen as the feedback variable. To ensure sinusoidal load voltage which faithfully tracks its reference signal, an outer feedback voltage loop is incorporated. The resultant control strategy applicable to the UPS and UIS is a current-regulated voltage-controlled scheme involving an inner feedback loop with the capacitor current and an outer loop with the capacitor voltage.

Selection of the controllers of the feedback loops is carried out using Bode diagram and time-domain error analysis. It is shown that proportional controllers in the feed-forward path of both the inner and outer feedback loops are sufficient to produce a system with excellent dynamic performance, and well-regulated and nearly perfect sinusoidal load voltage or utility line current. As a result, the proposed control scheme is simple to implement. Experimental verification of the proposed scheme for single-phase and three-phase UPS, and single-phase UIS is presented in the thesis to demonstrate the feasibility of the proposed control strategy, and the validity of the analytical models.

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Contents

Abstract	ii
Acknowledgments	iv
List of Figures	ix
List of Tables	xviii
1 INTRODUCTION	1
1.1 The Uninterruptible Power Supply	1
1.1.1 UPS System Specifications	2
1.1.2 UPS System Configurations	4
1.1.3 Control Schemes for Uninterruptible Power Supplies	16
1.2 The Utility Interactive System	26
1.2.1 The Line-Frequency Link UIS	28
1.2.2 The High-Frequency Link UIS	33
1.3 Thesis Objectives and Outline	37
2 The Single-Phase Voltage-Source Uninterruptible Power Supply System	40

2.1	General Model of the Single-Phase UPS Inverter	41
2.2	Time-Continuous Models of the UPS System	43
2.2.1	The Low-Frequency Model	45
2.2.2	Steady-State Analysis of the Low-Frequency Model	46
2.2.3	The High-Frequency Model	47
2.3	Selection of Filter Parameters	48
2.4	Small-Signal Dynamic Model	54
2.5	Selection of Feedback Control Scheme	58
2.5.1	Capacitor (Load) Voltage as Feedback Variable	59
2.5.2	Inverter Output Current as Feedback Variable	61
2.5.3	Capacitor Current as the Feedback Variable	68
2.5.4	The Proposed Control Scheme	70
2.6	Frequency Domain Analysis and Design of the Proposed Scheme	76
2.6.1	Frequency Domain Analysis of the Inner Current Loop	76
2.6.2	Frequency Domain Design of the Inner Current Loop	79
2.6.3	Frequency Domain Analysis of the Outer Voltage Loop	83
2.6.4	Frequency-Domain Design of the Outer Voltage Loop	83
2.7	Computer Simulation	86
2.8	Experimental Results of the Proposed System with Linear Loads	86
2.9	Experimental Results of the Proposed System with Non-Linear Loads	98
2.10	Summary	99
3	The Three-Phase Voltage-Source Uninterruptible Power Supply System	104
3.1	General Model of the Three-phase UPS Circuit	105

3.2	Low-Frequency Model in the Stationary Frame of Reference	109
3.3	Low-Frequency Model in the Rotating Frame of Reference	112
3.4	Linearized Model in the Rotating Frame of Reference	117
3.5	Steady-State Model and Analysis	121
3.6	Small-Signal Dynamic Model and Analysis	123
3.7	Incremental Dynamics in the Three-Phase UPS System	131
3.7.1	Incremental Dynamics of the Capacitor Voltage	131
3.7.2	Incremental Dynamics of the Capacitor Current	135
3.8	Computer Simulation of the Three-Phase UPS System	139
3.9	Experimental Verification	144
3.10	Summary	151
4	The Single-Phase Voltage-Source Utility Interactive System	153
4.1	Low-Frequency Model of the Single-Phase Utility Interactive Inverter	154
4.1.1	Steady-State Analysis of the Low-Frequency Model	156
4.1.2	Effect of the Filter Parameters on the Steady-State Operation of the UIS	157
4.2	Small-Signal Model of the UIS	160
4.2.1	Incremental Dynamics of the Power Circuit State Variables . .	162
4.2.2	Closed-Loop Operation of the UIS	164
4.3	Computer Simulation of the UIS	164
4.4	Experimental Results	166
4.5	Summary	173
5	The Three-Phase Voltage-Source Utility Interactive System	179

5.1	General Model of the Three-Phase UIS	179
5.2	Low-Frequency Averaged Model	183
5.3	Low-Frequency Model in the Rotating Frame of Reference	184
5.4	Linearized Low-Frequency Model	188
5.5	Steady-State Model and Analysis	192
5.6	Small-Signal Model and Analysis	194
5.6.1	Incremental Dynamics of the Utility Line Current	196
5.6.2	Incremental Dynamics of the Capacitor Voltage	202
5.6.3	Incremental Dynamics of the Capacitor Current	206
5.7	Computer Simulation	212
5.8	Summary	217
6	Summary and Conclusions	224
6.1	Suggestions for Future Work	228
	References	230
A	Control Circuit of the Proposed Control Scheme	244

List of Figures

1.1	Block diagram of the voltage-fed UPS system	5
1.2	The triport UPS system	7
1.3	The hybrid UPS system	9
1.4	Block diagram of the current-fed UPS system	10
1.5	The high-frequency link UPS configuration	12
1.6	The bilateral high-frequency link UPS configuration	14
1.7	The DC resonant link UPS configuration	15
1.8	Dead-beat control	21
1.9	Block diagram of the state-variable feedback scheme	23
1.10	Schematic diagram of the utility interactive system	27
1.11	Circuit diagram of the line-frequency link voltage-source utility interactive system	28
1.12	Circuit diagram of the flyback utility interactive system	31
1.13	Circuit diagram of the current-source UIS	32
1.14	Schematic diagram of the high-frequency link UIS	33
1.15	Circuit diagram of the high-frequency link voltage-source utility interactive system	34
1.16	The High-frequency resonant link UIS	36

2.1	Single-phase voltage-source UPS inverter with R-L loads	42
2.2	Circuit diagram of the steady-state low-frequency model	46
2.3	Waveshape of the dominant harmonic component in the inverter output voltage	49
2.4	Effect of filter parameters on the normalized filter ratings, attenuation, and THD of the load voltage	53
2.5	Root locus of the incremental dependence of the capacitor voltage due to incremental changes in the modulating signal at various loading conditions	60
2.6	Computer simulation results of the inverter output voltage and cur- rent of the single-phase UPS system with 0.7 pf lagging load and the capacitor voltage employed as the feedback variable	62
2.7	Computer simulation results of the load (capacitor) voltage and load current of the single-phase UPS system with 0.7 pf lagging load and the capacitor voltage employed as the feedback variable	63
2.8	Computer simulation results of the inverter output voltage and current of the single-phase UPS system with unity power factor load and the capacitor voltage employed as the feedback variable	64
2.9	Computer simulation results of the load (capacitor) voltage and load current the of single-phase UPS system with unity power factor load and the capacitor voltage employed as the feedback variable	65
2.10	Root locus of the incremental dependence of the inverter output current due to incremental changes in the modulating signal	66

2.11 Circuit model of the single-phase UPS system with the inverter output current employed as the feedback variable	67
2.12 Root locus of the incremental dependence of the capacitor current due to incremental changes in the modulating signal	69
2.13 Control of the single-phase UPS system employing the capacitor current as the only feedback variable	70
2.14 The proposed control strategy of the single-phase voltage-source UPS system	71
2.15 Computer simulation of the inverter output voltage and current employing the proposed control scheme	74
2.16 Computer simulation waveforms of the capacitor voltage and current in the single-phase UPS system employing the proposed control scheme	75
2.17 Bode plot of the open-loop transfer function of the inner current loop at various loading conditions	78
2.18 Closed-loop frequency response of the inner current loop with no-load	80
2.19 Closed-loop frequency response of the inner current loop with 0.75 pf lagging load	81
2.20 Closed-loop frequency response of the inner current loop with unity power factor load	82
2.21 Closed-loop frequency response of the inner current loop for 0.75 power factor load and $k_{pc}=2.0$	84
2.22 Bode plot of the open-loop transfer function of the outer voltage loop	85
2.23 Error in the magnitude and phase of the capacitor voltage with respect to its reference waveform for various values of k_{pv}	87

2.24	Time-domain simulation of the inverter output voltage and current of the proposed control scheme with $k_{pc}=2.0$ and $k_{pv}=2.75$	88
2.25	Time-domain simulation of the capacitor voltage and current of the proposed control scheme with $k_{pc}=2.0$ and $k_{pv}=2.75$	89
2.26	Time-domain simulation of the load current of the proposed control scheme with $k_{pc}=2.0$ and $k_{pv}=2.75$	90
2.27	Experimental waveforms of the steady-state inverter output voltage and current	92
2.28	Experimental waveforms of the steady-state capacitor voltage and load current	93
2.29	Experimental waveforms of the steady-state inverter output voltage and load voltage	94
2.30	Experimental waveforms of the steady-state capacitor voltage and current	95
2.31	Experimental waveforms of the transient response of the load voltage from "cold" start to full-load	96
2.32	Experimental waveforms of the dynamic response of the capacitor voltage for 100% step change in the load	97
2.33	Schematic diagram of the proposed scheme with non-linear load . . .	98
2.34	Experimental waveforms of the proposed scheme for non-linear loads with $C_f=100.0 \mu\text{F}$	100
2.35	Experimental waveforms of the proposed scheme for non-linear loads with $C_f=600.0 \mu\text{F}$	101
2.36	Experimental waveforms of the proposed scheme for non-linear loads with $C_f=900.0 \mu\text{F}$	102

3.1	Three-phase UPS circuit	106
3.2	Pole-zero map of the open-loop transfer function of the capacitor voltage for $z_l = 10.0\Omega$ at 0.7 power factor lagging load	128
3.3	Pole-zero map of the open-loop transfer function of the capacitor voltage for $z_l = 10.0\Omega$ at unity power factor load	130
3.4	Experimental verification of the frequency response of the open-loop transfer function of the capacitor voltage	132
3.5	Root locus of the incremental change of the capacitor voltage due to incremental variation in the modulating signal for $Z_l = 10.0\Omega$ at 0.7 power factor lagging load	133
3.6	Root locus of the incremental change of the capacitor voltage due to incremental variation in the modulating signal for $Z_l = 10.0\Omega$ at unity power factor load	134
3.7	Pole-zero map of $G_{icr}(s)$ for $Z_l = 10.0\Omega$ at 0.7 power factor lagging load	136
3.8	Root locus of the incremental change in the capacitor current due to incremental variation in the modulating signal at $Z_l = 10.0\Omega$ at 0.7 power factor lagging load	137
3.9	Root locus of the incremental change in the capacitor current due to incremental variation in the modulating signal for $Z_l = 10.0\Omega$ at unity power factor load	138
3.10	The proposed three-phase UPS system	140
3.11	Simulation waveforms of the DC side quantities of the power inverter	141
3.12	Simulation waveforms of the three-phase inverter output line-to-neutral voltage	142

3.13	Simulation waveforms of the three-phase inverter output current . . .	143
3.14	Simulation waveforms of the three-phase load voltages (line-to-neutral)	145
3.15	Simulation waveforms of the three-phase capacitor currents	146
3.16	Experimental waveforms of the load voltage	147
3.17	Experimental waveforms of the capacitor currents	148
3.18	Experimental waveforms of transient response of the load voltage . .	149
3.19	Experimental waveforms of the dynamics response of the load voltage	150
4.1	Power circuit of the utility interactive inverter	154
4.2	Low-frequency model of the UIS	156
4.3	Phasor diagram of the steady-state operation of the UIS	158
4.4	Relationship between the required magnitude of the fundamental component of the inverter output voltage and the power factor for various values of filter shunt capacitor.	159
4.5	Root loci of the incremental changes of the power circuit state variables due to incremental variations in the modulating signal	163
4.6	The proposed closed-loop single-phase voltage-source UIS	165
4.7	Inverter output voltage and current waveforms of the UIS at zero-leading power factor	167
4.8	Capacitor voltage and current waveforms of the UIS at zero-leading power factor	168
4.9	Utility voltage and line current waveforms of the UIS at zero-leading power factor	169
4.10	Inverter output voltage and current waveforms of the UIS at unity power factor	170

4.11 Capacitor voltage and current waveforms of the UIS at unity power factor	171
4.12 Utility voltage and line current waveforms of the UIS at unity power factor	172
4.13 Experimental waveforms of the inverter output voltage and current in the single-phase UIS at zero-leading power factor	174
4.14 Experimental waveforms of the capacitor voltage and current in the single-phase UIS at zero-leading power factor	175
4.15 Experimental waveforms of the utility voltage and current in the single-phase UIS at zero-leading power factor	176
4.16 Experimental waveforms of the utility voltage and current in the single-phase UIS at unity power factor	177
5.1 Circuit diagram of the three-phase voltage-source utility interactive system	180
5.2 Equivalent circuit model of the three-phase voltage-source UIS in the rotating frame of reference	189
5.3 Pole-zero map of the transfer function of the incremental variation in the utility current for unity power factor operation	198
5.4 Pole-zero map of the transfer function of the incremental variation in the utility current for zero-leading power factor operation	199
5.5 Root locus of the incremental variation in the utility line current for incremental changes in the control signal: unity power factor operation	200

5.6	Root locus of the incremental variation in the utility line current for incremental changes in the control signal: zero-leading power factor operation	201
5.7	Time-domain simulation of the utility line current with the utility line current i_u as the feedback variable: unity power factor operation . . .	203
5.8	Pole-zero map of the transfer function of the capacitor voltage for unity power factor operation	204
5.9	Pole-zero map of the transfer function of the capacitor voltage for zero-leading power factor operation	205
5.10	Root locus of the incremental variation in the capacitor voltage for incremental change in the control signal: unity power factor operation	207
5.11	Root locus of the incremental variation in the capacitor voltage for incremental change in the control signal: zero-leading power factor operation	208
5.12	Time domain simulation of the capacitor voltage with the capacitor voltage as the only feedback variable: zero-leading power factor operation	209
5.13	Root locus of the incremental variation of the capacitor current due incremental changes in the control signal: unity power factor operation	210
5.14	Root locus of the incremental variation of the capacitor current due incremental changes in the control signal: zero-leading power factor operation	211
5.15	Bode plot of the open-loop transfer function of the inner current loop	213
5.16	Bode plot of the closed-loop transfer function of the inner current loop for $k_{pc}=1.0$	214

5.17	Effect of k_{pc} on the Bode plot of the closed-loop transfer function of the inner current loop for unity power factor operation	215
5.18	The closed-loop three-phase UIS	216
5.19	Computer simulation waveforms of the three-phase inverter output current: unity power factor operation	218
5.20	Computer simulation waveforms of the three-phase line-to-neutral capacitor (load) voltage: unity power factor operation	219
5.21	Computer simulation waveforms of the three-phase capacitor currents: unity power factor operation	220
5.22	Computer waveforms simulation of the three-phase utility line current: unity power factor operation	221
5.23	Computer simulation waveforms of the three-phase utility voltage	222
A.1	Circuit diagram of the proposed control strategy for the single phase UPS system	245
A.2	Soft-start circuit	246
A.3	Block diagram of the carrier waveform generation	247
A.4	Block diagram of the logic circuit for dead-time generation	248
A.5	Timing diagram for dead-time generation	249
A.6	Photograph of the prototype three-phase UPS system	250
A.7	Photograph of the power sub-circuit of the prototype three-phase UPS system	251
A.8	Photograph of the control circuit of the prototype three-phase UPS system	252

List of Tables

3.1	Experimental verification of the steady-state values of the low-frequency model	151
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Chapter 1

INTRODUCTION

Optimum performance obtained by Pulse-Width Modulation (PWM) techniques has revolutionized the field of static DC to AC conversion. Implementation of these techniques has been facilitated by the advent of high-power transistors such as Insulated Gate Bipolar Transistors (IGBT) and power Metal Oxide Field Effect Transistors (MOSFET). These devices offer outstanding characteristics of high-power handling capabilities and very fast switching frequency.

This chapter presents a review of different circuit topologies and various control strategies employed in two widely used DC to AC conversion applications; namely the Uninterruptible Power Supplies (UPS) and the Utility Interactive Systems (UIS). The review will highlight the main advantages and disadvantages of each scheme. Finally, the thesis objectives and outline are presented.

1.1 The Uninterruptible Power Supply

Critical loads, such as medical instrumentation, process controllers, monitoring circuits and data processing systems (e.g. computers, communication systems, protection systems, financial transaction handlers, etc.), require continuity of energy

power supply, high-quality load voltage, and high rate of availability and reliability. These requirements dictate that a disturbance-free source of supply, other than from the local electric utility, is mandatory. This demand has been met recently by the Uninterruptible Power Supply (UPS).

In general, the UPS provides continuous energy power supply, and the total loss of power of the utility and the UPS system is usually kept within one complete cycle based on the utility frequency. Typically, the requirement of the high-quality load voltage for UPS systems is achieved by employing various control schemes which provide a load voltage with low distortion.

1.1.1 UPS System Specifications

The solid-state converter offers many features that makes it attractive for UPS applications. It is compact, reliable, and, depending on the control scheme employed, it generates very low or no audible noise. Thus, it becomes ideally suited for medical, communication and computer environments.

The performance characteristics that distinguish solid-state UPS systems from other static AC power supplies used in, for example, variable speed AC drives, are the “clean” and well-regulated AC output power. To achieve these performance characteristics, the UPS system should meet the following specifications [1, 2] :

1. The amplitude of the load voltage should be kept constant irrespective of the variations in the DC supply voltage level (typically specified as $\pm 10\%$ variation), or changes in the magnitude or power factor of the load. Fluctuation of the critical load voltage could result in permanent damage to the critical load.
2. The load voltage should be of high quality. The total harmonic distortion

(THD) of the load voltage should be less than 5 %. The concept of high-quality load voltage expresses the relative harmonic content in the load voltage and a stable output voltage independent of the pollution on the utility network.

3. The frequency of the load voltage should be kept constant. This condition is essential for critical loads with an AC-DC adaptor. The load adaptor is usually provided with a DC filter whose components are optimally chosen to minimize its size for nominal supply frequency and amplitude. When the supply frequency deviates from its nominal value, the load filter components become ineffective in producing a well-regulated and "clean" DC output voltage.
4. The system should provide continuous energy supply. Typically, the maximum permissible duration of total loss of load voltage for computer applications is 16 milli seconds, after which loss of memory of data takes place. The system batteries should have sufficient ampere-hour rating to maintain the UPS output for a specified time (usually 30 min.) to allow for data saving and proper shut-down procedures of the computer system.
5. The UPS system should have fast transient response. Systems with sluggish response to either load changes or supply variations could lead to malfunction of the critical load. In some UPS systems (e.g. the stand-by UPS), the system response to the local utility disturbances should be fast with small transfer time.

The above specifications have been met in the solid-state UPS system through improvements in system topology and control strategies.

1.1.2 UPS System Configurations

Since its introduction in 1965, the solid-state UPS system has undergone several topological evolutions. In broad terms, UPS systems may be classified as on-line and stand-by systems. In on-line systems, the load is constantly supplied by the utility through the UPS system. Thus, on-line systems provide “clean” and well-regulated AC power to the critical load and protect the load from utility disturbances such as transients or brown outs. On the other hand, in stand-by systems, the load is supplied by the raw AC line while the UPS inverter may be in an idle or OFF condition. When the loss of the utility line voltage is detected, the inverter is brought on-line via a transfer switch. The stand-by system is a redundant system, and hence, provides higher reliability and efficiency. However, it requires a finite transfer time for the stand-by equipment to be brought on-line to supply the critical load with regulated power. A methodology for rating the output response quality of a backup power supply based upon the units ability to maintain acceptable output voltage before, during, and after the transfer to battery power has been reported in [3].

Both the on-line and the stand-by UPS systems may employ the same type of converter-inverter configuration. Consequently, they are further classified according to the power conversion stage. Presently, uninterruptible power supplies can be categorized into four main configurations as follows:

- voltage-fed UPS,
- current-fed UPS,
- high-frequency link UPS, and
- DC resonant link UPS.

The Voltage-Fed UPS Configuration

The voltage-fed UPS system is the most widely used UPS system configuration [4]-[8]. Figure 1.1 shows the block diagram of the on-line voltage-fed, or the conventional, UPS system. It consists of an input stage (usually controlled bridge rectifier), a low-pass input filter, a battery bank, a switching inverter, a low-pass output filter, an isolation transformer, and a static bypass switch.

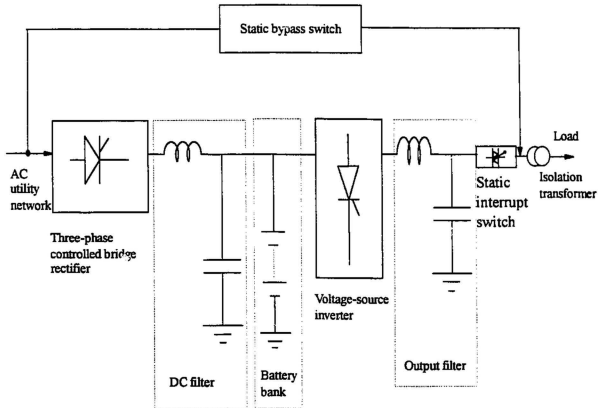


Figure 1.1: Block diagram of the voltage-fed UPS system

The function of the input stage is to convert the AC supply voltage into DC voltage at different levels. The level of the DC voltage of the input stage is regulated

using conventional control schemes such as phase angle control [9]. Alternatively, regulation of the DC bus can be achieved using more sophisticated schemes such as the switched mode rectifier [10], or the high-frequency link DC to DC converter [11]-[14]. The DC voltage at the output of the input filter charges a bank of batteries as well as provides the voltage source for the switching inverter. The battery bank is kept floating, and in case of an AC line power failure, the battery bank supplies the load through the switching inverter. When the utility line recovers, the controlled bridge rectifier recharges the batteries and supplies the load through the switching inverter. The switching inverter converts the DC voltage into AC using a conventional pulse-width modulation scheme (PWM). The output filter provides further attenuation of the output harmonics so as to provide a load voltage with low harmonic content.

In the event of failure in the converter-inverter system, the load is supplied directly from the utility line through the static bypass switch. This emergency situation is not recommended for long duration of load operation.

As discussed above, in the normal operation of the voltage-fed UPS, the critical load is continuously supplied with the electrical energy from the utility via the converter-inverter system. This feature has the advantage of protecting the load from momentary disturbances, such as voltage and frequency fluctuation, brown outs, transients, etc ..., on the utility network. In other words, this system provides an uninterrupted and disturbance-free supply to the critical load.

One of the drawbacks of the voltage-fed UPS system is that the system output voltage is prone to have a DC component due to the ripple on the DC link voltage [15]. A significant level of the DC component at the inverter output could result in saturating the isolation transformer. This drawback can be overcome by using a

relatively large DC filter at the inverter input.

A stand-by version of the voltage-fed UPS system, the triport UPS system, which incorporates additional elements to regulate the utility voltage is shown in Fig. 1.2 [16]. In normal operation, the load is constantly supplied from the utility source

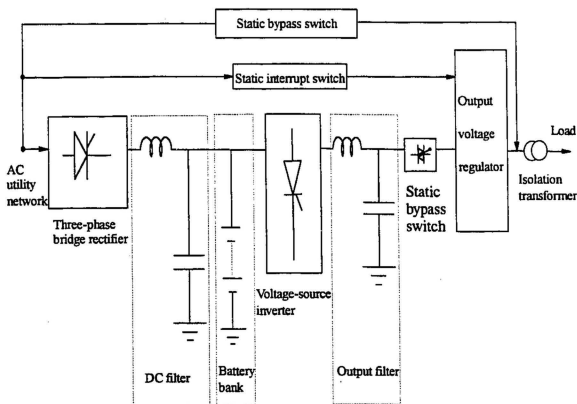


Figure 1.2: The triport UPS system

through an automatic voltage regulator (AVR). The AVR is normally a transformer with two primary windings; one winding is fed by the AC line while the other is supplied by the inverter. The transformer output voltage is regulated by tuned filters and thyristor-controlled reactor arrangement. The UPS inverter is maintained in a

“hot” stand-by condition, and when the AC line fails, it provides the critical load with the required power. Such power flow arrangement is justified because it ensures that the static inverter path remains operational and ready to deliver full power instantaneously whenever needed.

If the utility supply deviates from its specified limits for a certain duration of time (typically 20 ms), the static interrupt switch is switched OFF, and full-load power is supplied by the DC batteries through the static inverter. In the event of failure in the static inverter or the AVR, the critical load is supplied directly by the utility line through the bypass switch. In some cases, the system bypass switch is chosen to be a non-static switch. This prevents the critical load from being subjected to high voltage transients that can pass through a static switch.

The triport configuration has the advantage of lower cost: the rating of the bridge rectifier is low because it is used only to trickle charge the battery bank. On the other hand, the scheme does not provide adequate protection of the load from the utility network transients. The output transformer is also large because of the multiple primary windings. Furthermore, the system suffers from instability phenomena at light loads. A conventional approach to solving this problem is to apply dummy loads at the transformer output. This approach has an adverse impact on the system efficiency. Alternatively, an active filter circuit may be used to provide stable control of the AVR [17].

In order to overcome the instability problems associated with the triport systems, the AVR is replaced by a synchronous motor-generator set. The result is the stand-by hybrid configuration shown in Fig. 1.3 [18]. Under normal operating conditions, the utility supply provides about 95 % of the power required by the critical load via

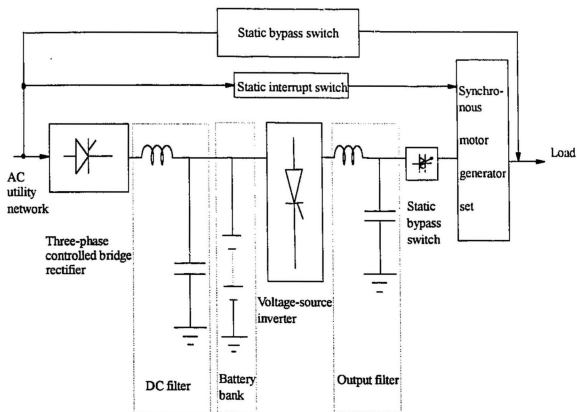


Figure 1.3: The hybrid UPS system

the static interrupt switch and the motor-generator set, with the conventional UPS system providing the rest of the load power.

The hybrid configuration offers high reliability and efficiency. However, the system requires complex control circuitry. For example, to adjust the level of power flow in the system buses, a special synchronization circuit is required. Overall, the system size is large and its noise level is higher than the conventional static UPS system. Moreover, it is very expensive and can only be economically considered for large loads.

Control and operation of distributed UPS systems, which employ the basic voltage-source UPS configuration for large/flexible loads, have been investigated in [19]-[21]. Distributed UPS systems have high reliability and permit critical loads to be fed from various UPS units along various paths.

The Current-Fed UPS Configuration

The conventional current-fed UPS system is shown in Fig. 1.4. It consists of an

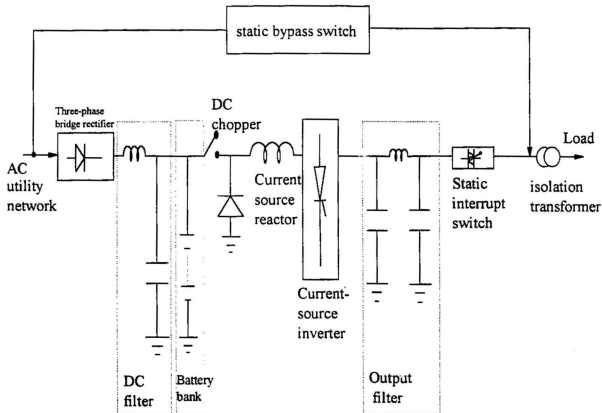


Figure 1.4: Block diagram of the current-fed UPS system

uncontrolled bridge rectifier, a low-pass input filter, a battery bank, a DC chopper,

a smoothing reactor, a PWM current-source inverter, an output filter, an isolation transformer and a static bypass switch.

The unregulated DC voltage at the output of the DC filter is converted to a current source by the large current-source reactor. The DC chopper is used to control the level of the current source to ensure constant output voltage irrespective of load or supply changes. Alternately, the control of the DC current level can be achieved by replacing the uncontrolled bridge rectifier and the DC chopper by a controlled bridge rectifier.

The function of the current-source inverter is to convert the input DC current into an AC current. The output filter arrangement provides attenuation of the output current harmonics and also reduces the voltage spikes associated with the current-source inverter switching, and hence the stresses on the switching devices [15]. In order to improve the power factor of the input stage and obtain higher overall efficiency of the system, a bilateral current-fed system with variable output frequency was proposed in [22]. Recently, a digitally controlled current-source inverter-based UPS system, which constructs the sinusoidal load voltage from information available from the system DC bus, has been proposed in [23].

Since the current-source reactor converts the DC-link voltage into a current source, the current-fed UPS system is immune to DC components in its output voltage. However, it requires an extra power conversion stage (i.e., the DC chopper and the current-source reactor) to create the controllable current source. The large current-source reactor results in a system with slower dynamic response.

The High-Frequency Link UPS Configuration

Figure 1.5 shows the block diagram of the high-frequency link UPS system [24]. It

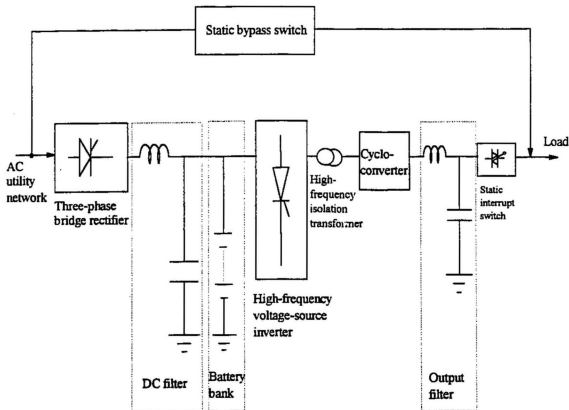


Figure 1.5: The high-frequency link UPS configuration

consists of a controlled-bridge rectifier, a low-pass input filter, a DC battery bank, a high-frequency voltage-source inverter, a high-frequency isolation transformer, a cycloconverter, a low-pass output filter, and a static bypass switch. The functions of the bridge rectifier, the low-pass input filter and the battery bank are the same as those described for the previous UPS systems.

The output of the high-frequency inverter is a pulse-width modulated AC voltage

switched at very high frequency (typically 20 kHz). A sinusoidal output voltage of the UPS system, whose frequency is the same as the supply frequency, is then synthesized from the inverter output voltage using a cycloconverter. The undesired harmonics at the cycloconverter output are suppressed by the low-pass filter at the load terminals.

The high-frequency UPS scheme offers several improved performance features over the conventional voltage-fed and current-fed UPS systems. Since the inverter is switched at very high frequency, the size of the isolation transformer is significantly reduced. Moreover, the level of audible noise produced by the isolation transformer is also reduced. However, these desirable features are achieved at the expense of increased number of switching devices, complex control circuitry, and hence, a reduction in the system reliability. A major problem with the system is the commutation of the cycloconverter which is load dependent and ineffective under certain load conditions. Moreover, using two power conversion stages (high-frequency inversion and cycloconversion) adversely affects the system efficiency. Furthermore, when the inverter fails, the critical load is supplied from the raw utility voltage via the bypass switch without isolation.

A stand-by version of the high-frequency link UPS is shown in Fig. 1.6 [25]. In normal operation, the critical load is supplied from the power grid through an isolation transformer. Meanwhile, the battery bank is charged through the cycloconverter, the high-frequency isolation transformer, and the high-frequency PWM inverter. In case of power grid failure, the power delivered to the critical load is drawn from the battery bank by reversing the direction of power flow in the high-frequency link system.

This system has higher efficiency because of the elimination of the input AC-to-DC conversion stage. However, it has the disadvantage of imposing finite transfer

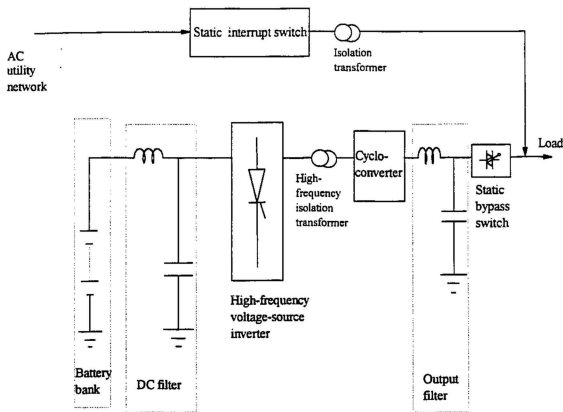


Figure 1.6: The bilateral high-frequency link UPS configuration

time to change from rectification mode to inversion mode and provide well-regulated power when needed by the critical load. To achieve successful operation, the system control scheme has to be carefully designed to avoid long transfer times.

The DC Resonant Link UPS System

DC resonant link converters were first proposed for AC motor drive applications [26]-[28]. In this scheme, the DC bus voltage is made to oscillate at very high frequency by incorporating a resonant circuit in the input DC voltage stage. The inverter switching

devices are turned ON/OFF at the zero-voltage points of the DC bus, hence achieving zero-switching losses.

A single-phase version of the DC resonant link UPS system is shown in Fig. 1.7 [29]. The switches of the full-bridge inverter are controlled to produce a three-level

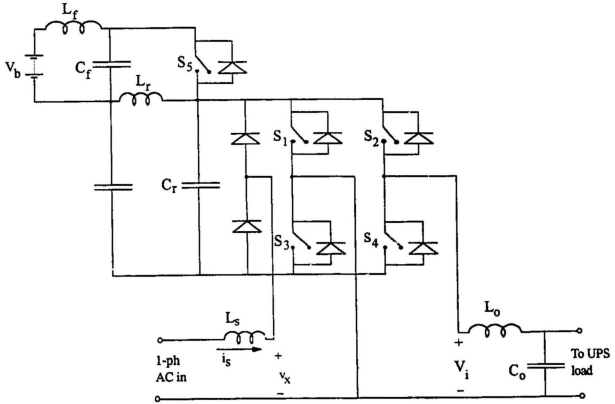


Figure 1.7: The DC resonant link UPS configuration

waveform at the inverter output; i.e., negative, zero, or positive voltage. The zero-voltage state can be achieved by either turning ON S_1 and S_2 or S_3 and S_4 . By employing this extra degree of freedom, the AC supply current can be actively shaped to follow a reference waveform. For example, switching S_1 and S_2 ON to realize a

zero voltage at the load terminal results in $v_x = 0$, while switching S_3 and S_4 ON produces the DC bus voltage across v_x . For a positive AC supply voltage, v_x causes the source current, i_s , to increase or decrease and vice versa when the AC supply voltage is negative.

This system is capable of simultaneously shaping the load voltage and the AC supply source current to follow their respective reference waveforms, thus eliminating the need for the input AC to DC conversion stage. Hence, the system has high efficiency. In addition, the system is capable of producing a load voltage that is higher than the DC bus voltage. However, the scheme has drawbacks that are common to this class of resonant converters: the regulation of the DC bus voltage requires complex control circuitry [30], and, the oscillation of the DC bus voltage is significantly high resulting in higher-order voltage harmonics superimposed on the AC supply voltage.

1.1.3 Control Schemes for Uninterruptible Power Supplies

The evolution in UPS system configurations has resulted in improved system efficiency and reliability. However, improvements in the system performance in terms of the system providing constant load voltage and frequency, high-quality load voltage, fast transient response, and reduced component size have been achieved through various modulation and control schemes employed in the inverter of the UPS system. In this section, a review of the different pulse-width modulation and control techniques currently employed in inverters is provided.

Pulse-width modulation (PWM) is a process through which a sinusoidal waveform can be synthesized from a train of positive and negative pulses with their widths varying according to certain modulation criteria. The purpose of using modulation tech-

niques for UPS systems is to control the amplitude of the load voltage and minimize the low-order harmonic contents of the output voltage.

The earliest PWM technique applied to UPS systems is the single pulse-width modulation scheme. This scheme is capable of load-voltage regulation and minimization of few selected harmonics in the inverter output. However, it requires large filter size and, as a result, there is an appreciable voltage drop across the filter series inductor. This voltage drop could reach as high as 40 % of the fundamental component of the inverter output voltage during switching in/out of the load [1]. Several years of research in this area have resulted in the development of modulation schemes that provide outstanding improvement in UPS system performance. The most widely used schemes can be listed as:

- sinusoidal pulse-width modulation,
- programmed optimum pulse-width modulation scheme,
- delta pulse-width modulation scheme, and
- real-time feedback control.

Sinusoidal Pulse-Width Modulation

Sinusoidal pulse-width modulation (SPWM) is a very popular scheme for both adjustable speed AC drives [31, 32] and UPS systems [2, 8, 15]. The manner of generating the switching points depends on the method of implementation of the modulation technique, and may thus be classified as natural and uniform sampling techniques.

In the naturally sampled SPWM, a triangular carrier wave is compared with a modulating reference signal and the natural points of intersection determine the

switching points for the inverter switching devices [33]. The distribution of the undesired harmonics depends on the frequency ratio of the carrier signal to the modulating signal. The higher the frequency ratio, the greater the “gap” between the fundamental component and the dominant harmonics. The SPWM scheme has the advantage of generating well-defined frequency spectrum of the inverter switching pattern, thus making it easier to design an optimum load filter to remove the undesired harmonics.

The uniform sampling method is based on the sample and hold principle. In this scheme, the sine modulating signal is replaced by an equivalent stepped signal. This technique is popular in microcomputer implementation [34]-[36]. The uniform sampling technique has the advantage of producing symmetrical pulses about the trough of the carrier wave. Thus, no sub-harmonics exist in the frequency spectrum of the inverter output voltage.

The Programmed Optimum Pulse-Width Modulation Scheme

The programmed optimum pulse-width modulation scheme, [14], is the most widely used scheme in the group of selected harmonic elimination techniques [37]-[39]. The switching instances of the inverter output pulses, which result in the elimination of selected order of harmonics or maximizing a performance criteria (such as voltage utilization), are determined a priori by solving a set of non-linear equations which describe the inverter output voltage waveform. The scheme, therefore, has the disadvantage of being computationally intensive and requires off-line calculations.

In UPS applications, the programmed inverter switching pattern is fixed [14]. The control of the magnitude of the load voltage is therefore achieved via the control of the front end AC-to-DC rectifier in both voltage-fed and current-fed configurations.

Although this technique attenuates the low-order harmonics and results in small filter size, it is characterized by slow dynamic response. Moreover, because the programmed inverter switching pattern is determined on the basis of the steady-state operation of the system, the performance of the UPS during transient stages and abnormalities is adversely affected.

The Delta-Modulation Scheme

Delta-modulation scheme was first introduced for digital communication networks, [40, 41], and later on for AC drives applications [42]-[45]. Among various delta-modulation strategies, the rectangular-wave delta-modulation (RWDM) scheme has gained increasing popularity for static PWM inverters [42]-[44, 46].

The RWDM is one of the simplest known methods of converting an analog signal into a digital format, and has been successfully implemented for UPS systems [46]. It has the advantage of very simple circuit implementation and the ability to produce sinusoidal load voltage with small filter parameters and moderate switching frequency. However, it suffers from the same drawbacks common to the class of hysteresis controllers, such as variable switching frequency [47]. The problem with variable switching frequency is that it generates a random and uneven switching pattern which stresses the power switching devices. Moreover, the frequency spectrum of the inverter output voltage contains frequency modulated components which interfere with communication equipment external to the power circuit. A synchronization technique to produce a fixed switching pattern at the output of the delta modulator using phase-locked loop circuit as a frequency multiplier has been proposed in [48]. However, the resulting control circuitry is complex and the main advantage of delta

modulators, namely, simple circuit implementation, is lost.

The Real-Time Feedback Control

In recent years much effort has been concentrated on the development of various real-time feedback control strategies for UPS applications. The widely used strategies for UPS can be listed as:

- dead-beat control,
- variable-structure control with sliding mode,
- state-variable feedback control, and
- current-regulated control.

The Dead-Beat Control

The principle of the dead-beat control scheme is illustrated with the aid of a voltage-source UPS inverter with a resistive load in Fig. 1.8 [61]. A feedback signal of the load voltage is employed in a dead-beat control algorithm to calculate the duration of the ON/OFF states of the inverter switching devices. Based on the measured signals at the instant $k-1$, the power circuit state variables are estimated at the next instant k using a state estimator. The state variables are then employed in a control algorithm which insures that the capacitor voltage is exactly equal to the reference voltage at the next sampling instant.

The dead-beat control scheme has been implemented successfully in single-phase and three-phase UPS systems in which the control algorithm relies on the value of the

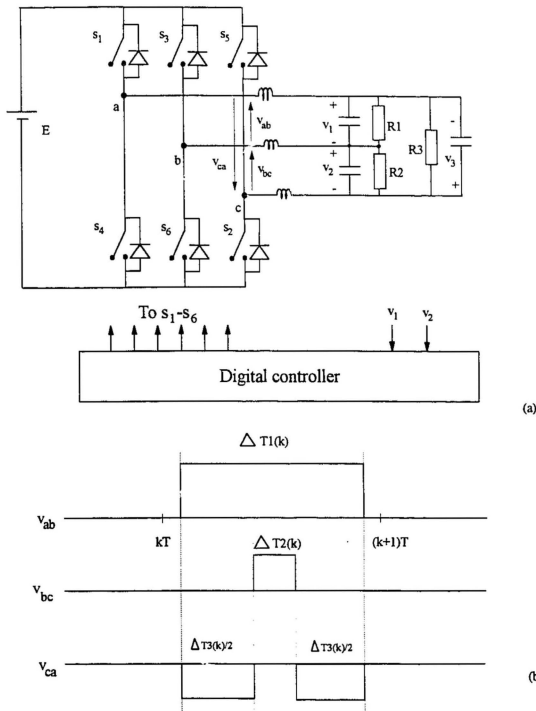


Figure 1.8: Dead-beat control: a) Schematic of the power circuit, b) Timing diagram

load resistance to estimate the circuit state variables [62]. This renders the system sensitive to parameter variations.

To overcome this problem, the disturbance observer-based dead-beat control was proposed in [63]. In this scheme, the inverter switching frequency is assumed to be sufficiently high so that the load current is modeled as a constant current over a switching interval. The load current is employed as a feedback variable in the state estimation algorithm to determine the state variables of the power circuit.

Although the disturbance observer-based dead-beat control has been shown to be compatible for both linear and non-linear loads, it is complex to implement. The scheme is even more difficult to implement at high-switching frequencies because of the need for a powerful microprocessor [64].

The State-Variable Feedback Control

The state-variable feedback technique is a well-established scheme in control systems literature [65]. Figure 1.9 shows the basic block diagram of the scheme. The system state variables, $\mathbf{X}(s)$, are sensed and multiplied by a gain matrix \mathbf{K} . Depending on the design of the gain matrix, closed-loop poles of the resultant system can be arbitrarily placed anywhere in the s -plane, thus, tailoring the complete system transient response. It is assumed that all the state variables are accessible for measurements. If any of the state variables is not accessible, such as in the case of AC drives, the state variable can be constructed using state-estimation algorithms [66].

In UPS applications, where all the system state-variables are available for measurement, it has been demonstrated recently that the scheme has good dynamic response and is capable of shaping the complete system transients [67]. However, the placement

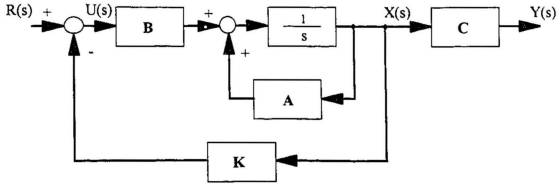


Figure 1.9: Block diagram of the state-variable feedback scheme

of the system poles at predetermined locations in the s -plane is costly; a dedicated digital signal-processing board to calculate optimum elements of the gain matrix is needed, and the number of sensors required is equal to the number of state variables to be controlled. For example, in a three-phase UPS system with a second-order filter and R-L load, six current sensors and three voltage sensors are required. Besides, the scheme is highly sensitive to load variations, making the computed elements of the gain matrix less than optimal.

The Variable-Structure Control with Sliding Mode

Variable structure control is a special type of control technique that is capable of making a control system very robust and insensitive to parameter variation and external disturbances. The control scheme was pioneered in the Soviet Union in the early 1950's [68]. The scheme was introduced for the control of systems where the right-hand side of the differential equation governing the system is not analytical,

such as in ON/OFF regulators [69, 70].

Variable structure control with sliding mode has gained attention recently in power switching converters where it is referred to as sliding mode control because the system state trajectory is forced to slide along a switching surface for any load conditions or external disturbances. Sliding mode control has been successfully implemented in a variety of motor drives [71]-[76].

Although the scheme has been shown to give fast dynamic response in voltage-source UPS inverters, it requires very high-switching frequency to avoid chattering problems [77]. Consequently, the overall system efficiency is reduced. Moreover, similar to the state-variable feedback control scheme, the sliding mode control requires high count of state-variable sensors.

Discrete versions of the sliding mode control for UPS applications with resistive loads have been shown to have fast transient and dynamic responses [78, 79]. However, the sampling process involved elevates the chattering problem.

The Current-Regulated Control

Current-regulated voltage-source PWM inverters have gained considerable attention over the past two decades. Various types of current-regulated controllers have been proposed in the literature for AC drives applications and static power supplies [49]-[60].

The control scheme configuration of current-regulated inverters has the general structure of inner-current and outer-voltage feedback loops. As a result, the scheme has fast dynamic response. In UPS applications, the filter capacitor current [56, 57] or the inverter output current [58, 59] is used as the feedback variable in the inner current

loop. The control algorithm either employs hysteresis controller or PWM schemes to generate the inverter switching pattern. Hysteresis controllers have the advantages of simplicity, fast dynamic response and robustness. However, they suffer from the same disadvantages mentioned earlier for delta modulators. These disadvantages can be overcome by using fixed-switching frequency, variable-duty cycle schemes.

In current-regulated schemes which use the inverter output current as the feedback signal, the reference current signal is obtained from the sum of the reference signal of the capacitor current and the actual load current. Simulation results have shown that this scheme is capable of producing load voltage with extra low total harmonic distortion [58]. Major drawbacks of the scheme are the high switch count and the use of high-switching frequency (in the order of 20.0 kHz).

1.2 The Utility Interactive System

Renewable energy sources (RES) have gained increasing interest as an alternative source of electrical energy. They are abundant, free, inexhaustible, and environmentally friendly.

Renewable energy sources such as wind mills and photo-voltaic systems require load leveling to extend the period of operation throughout the user's daily demand. One way to achieving this load leveling is to use DC battery bank or flywheels as local energy storage. In general, the output current/voltage of the renewable energy source is uncontrolled, and a power conditioning unit is usually employed to interface the RES to the load. The power conditioning unit may operate in the stand-alone mode. This approach is widely used at remote sites which are not served by the public power grid. When the renewable energy source is connected to the utility network, through the power conditioning unit, the electric distribution system can be used to absorb the excess power generated by the renewable energy source. During RES down times, the utility network supplies the user's demand. In this configuration, the power conditioning unit is referred to in the literature as the utility interactive system (UIS).

Figure 1.10 shows a block diagram representation of a UIS. The utility interactive system typically consists of an uncontrolled rectifier, AC-to-DC inverter and an output filter. The uncontrolled bridge rectifier is used when the output of the renewable energy source is AC, as in the case of induction generators [80]. The power inverter employed is typically a line-commutated inverter with harmonic filter at the output to improve the quality of the utility line current. The line-commutated inverter has the disadvantage of requiring a large DC choke, expensive and bulky harmonic filters,

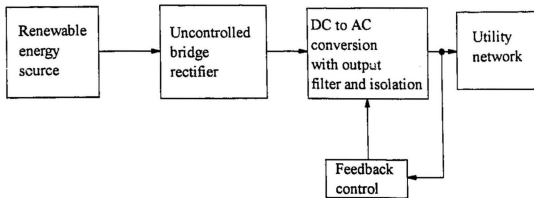


Figure 1.10: Schematic diagram of the utility interactive system

and modest total harmonic distortion of the line current. Present standards require that the total harmonic distortion of the current fed into the utility network should be less than 5%, with individual harmonics not exceeding 3% [81]. During the past fifteen years, much effort has been concentrated on the development of switch mode power conditioning topologies and switching strategies to meet the requirements of high-quality utility line current, and stable operation over a wide range of system conditions.

Utility interactive systems may be classified according to how the power conditioning unit is connected or linked to the utility network. The widely used connection schemes can be listed as:

- line-frequency link UIS, and
- high-frequency link UIS.

The inverter used in the line-frequency link scheme may be of the voltage-source or current-source type, while only voltage-source inverters are used in the high-frequency link. The voltage-source configuration requires closed-loop control operation to make

the output current of the UIS follow a reference sinusoidal waveform. In the current-source configuration, the output current of the UIS is shaped to follow a reference sinusoidal waveform using open-loop control scheme.

1.2.1 The Line-Frequency Link UIS

A single-phase voltage-source line-frequency link utility interactive system is shown in Figure 1.11 [81, 82]. It consists of an input capacitor filter, C_d , a single-phase voltage-source full-bridge inverter, and an output line inductor filter, L_f . Isolation

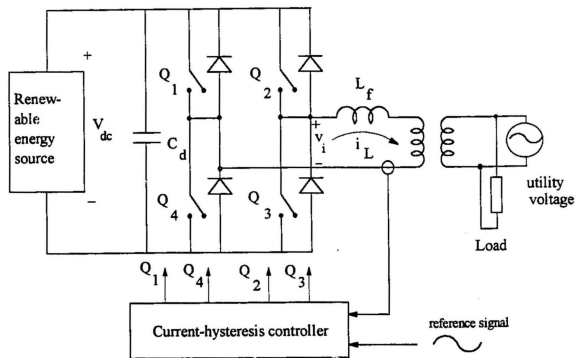


Figure 1.11: Circuit diagram of the line-frequency link voltage-source utility interactive system

from the utility line network is provided by a line-frequency transformer.

To meet the harmonic distortion requirements, the line current is made to faithfully follow a reference sinusoidal waveform. This is achieved by sensing the line current and comparing it with a reference sinusoidal waveform to generate a PWM pattern according to a certain control strategy, such as the hysteresis controller [82]. Alternatively, the PWM pattern can be generated without the need for a current sensor by employing a model-reference-adaptive based delta-modulation scheme [83]. The PWM waveform controls the appropriate switching devices in the power inverter such that the utility line current follows the reference sinusoidal waveform within a predetermined hysteresis window.

The system is capable of generating sinusoidal line current at any power factor with respect to the utility voltage. It has fast dynamic response and simple power and control circuit implementation. However, the control scheme generates an uneven and random PWM switching pattern which causes variations in the inverter switching frequency as the line current waveform changes. Consequently, the inverter output switching pattern is not only pulse-width modulated but also frequency modulated [47, 52]. The frequency-modulated nature of the inverter output switching pattern causes difficulties in synchronizing the inverter output current with the utility voltage. To overcome this difficulty, the current in the power circuit has to be reset to zero at every half cycle of the utility voltage. This is achieved by turning all switching devices in the power inverter OFF well before the zero-crossing of the utility voltage to allow the line current to decay to zero. The effect of the resetting process is an increase in the harmonic content of the utility line current.

The frequency modulation component in the inverter output voltage can be re-

duced by using a current-hysteresis controller with variable window width [84]-[86], or using a phase-locked loop delta-modulation controller [48]. The main drawback of these techniques is the resulting complex control circuit implementation.

Figure 1.11 shows that this control technique relies solely on the feedback signal of the inverter output current to control the wave shape of the utility line current. Consequently, the presence of filter elements on the AC side can cause disturbances which may lead to uncontrolled oscillations [87]. These uncontrolled oscillations cause fluctuations in the load voltage, and, if significant amplitude of oscillations occur, an overall system malfunction may take place. Passive damping techniques may be used to suppress such oscillations.

The line-frequency link is basically a step-down DC-to-AC converter. In other words, the maximum value of the fundamental component of the inverter output voltage is equal to the level of the DC input voltage. Thus, the system can operate properly only if the output voltage of the RES is greater than or equal to the utility voltage. For a utility voltage higher than that of the RES, the utility current becomes distorted. This problem is overcome by using a flyback converter configuration with fixed switching frequency and variable duty cycle control scheme [88].

Not only does this system overcome the problem of low voltage level at the output of the RES, it also circumvents the problems associated with the variable switching frequency of the hysteresis/delta controllers. The scheme employs the state-feedback control technique to stabilize the utility interactive system and shape the utility line current [89]. In addition, the scheme can only feed current at unity power factor with respect to the utility voltage. A major limitation of the flyback converter system is the complexity of the control circuit implementation.

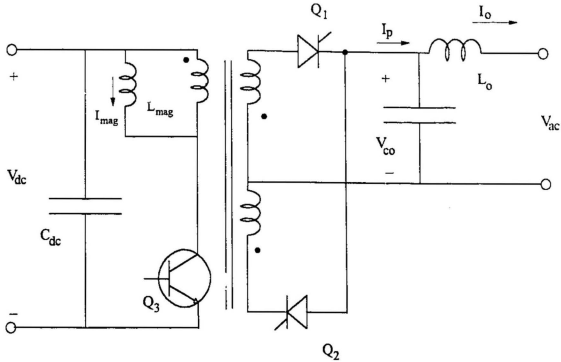


Figure 1.12: Circuit diagram of the flyback utility interactive system

The current-source version of the line-frequency link UIS is shown in Fig. 1.13. The output voltage of the RES is first converted to a current source using a large current-source reactor (CSR). The output capacitor, C_f , performs the double function of providing the output filtering with L_f and reducing the switching stresses of the switches $S_1 \dots S_4$. S_5 and S_6 are commutation switches which are used to provide an alternate path for the current flow during commutation and to avoid open circuit conditions at the output of the current-source reactor. The utility line current is shaped to follow a sinusoidal waveform by using an appropriate pulse-width modulation strategy. Thus, the UIS virtually operates in an open-loop control fashion

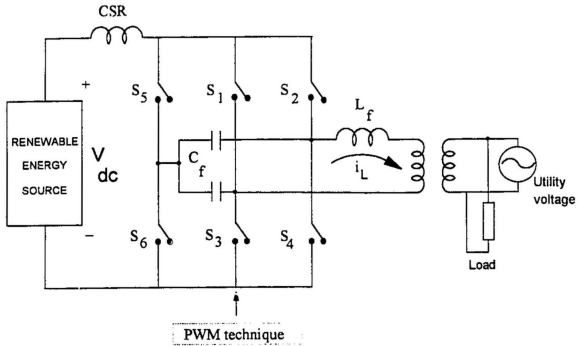


Figure 1.13: Circuit diagram of the current-source UIS

and feedback signals are only needed to adjust the output power level and synchronize the inverter output current with the utility voltage. The sinusoidal pulse-width modulation schemes have been used to implement the single-phase and three-phase current-source inverter-based UIS [90, 91].

In contrast to the voltage-source inverter, the current-source inverter is immune to short circuit faults that may take place at the output of the inverter circuit. However, the relatively large reactor results in a bulky system with slow dynamic response. In addition, the system requires extra power switching devices to circumvent open circuit conditions in the power circuit.

1.2.2 The High-Frequency Link UIS

The high-frequency link UIS was proposed primarily to overcome the problems of size, cost, and weight of the line-frequency link UIS [92]. The basic schematic of the high-frequency link concept is shown in Fig. 1.14. The most popular configuration

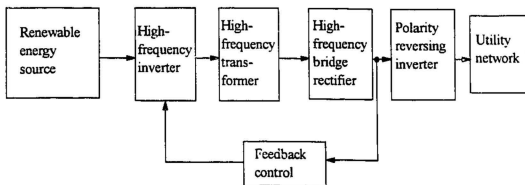


Figure 1.14: Schematic diagram of the high-frequency link UIS

and control scheme of the single-phase high-frequency (HF) link voltage-source utility interactive system is shown in Fig. 1.15 [93, 94]. The system employs a high-frequency bridge inverter, operating at approximately 10-16 kHz to invert the DC voltage at the output of the renewable energy source into a PWM high-frequency AC voltage. The AC voltage at the output of the HF bridge inverter is rectified via the HF isolation transformer and the HF bridge rectifier. A line-commutated, polarity-reversing inverter unfolds the rectified current waveform in the DC link inductor, L_d , and feeds it into the utility network.

The control of the utility line current relies on sensing the current in the DC link inductor, i_d and comparing it with a fraction of the rectified waveform of the utility voltage in a hysteresis comparator. The appropriate devices of the high-frequency in-

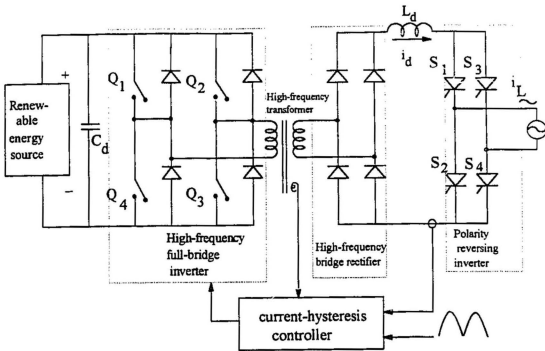


Figure 1.15: Circuit diagram of the high-frequency link voltage-source utility interactive system

verter are turned ON/OFF to force the link current, i_d , to follow a rectified sinusoidal waveform within the hysteresis window of the current-hysteresis controller. Due to the high switching frequency operation of the front-end inverter, the resulting utility line current is sinusoidal with very low harmonic content thus eliminating the need for a filter at the utility side.

The main advantage of the system is the reduction in the size and weight of the isolation transformer and of the system audible noise. This advantage is achieved at the expense of significant increase in the number of power semiconductor devices, and hence system cost, high switching losses, complex control circuitry, and lack of

capability of feeding or absorbing reactive power into/from the network.

A variation of the high-frequency link scheme employs a push-pull inverter and a high-frequency center-tapped transformer [95]. The utility line current is used in a fixed-switching frequency, variable-duty cycle scheme to control the shape of the utility line current. This system has the advantage of reducing the number of HF switching devices and eliminating all the disadvantages associated with hysteresis controller. To accommodate large variations in the output voltage of the renewable energy source, a DC-to-DC boost converter is employed at the front-end to interface the RES to the utility interactive system [96].

Recently, the DC-to-DC resonant conversion concept has been proposed for the inverter switching to reduce the high switching losses associated with the high-frequency inverter discussed above. Figure 1.16 shows one of the circuit configurations of the high-frequency link UIS in which the PWM inverter is replaced by a high-frequency resonant inverter [97]-[99]. The switches of the high-frequency resonant inverter are turned ON/OFF at a switching frequency slightly higher than the resonant frequency such that the DC link current is made to follow a rectified sinusoidal waveform.

The high-frequency resonant link concept allows high switching frequencies to be used resulting in low audible noise. However, in addition to the drawbacks previously mentioned for the HF link UIS, there is a significant increase in the losses and VA ratings of the resonant circuit. Also, the switching devices of the high-frequency inverter experience significant voltage stresses because of the high voltages developed across the elements of the resonant circuit.

A close examination of the current technology for UIS applications shows that although all the above schemes result in a sinusoidal utility line current, they are

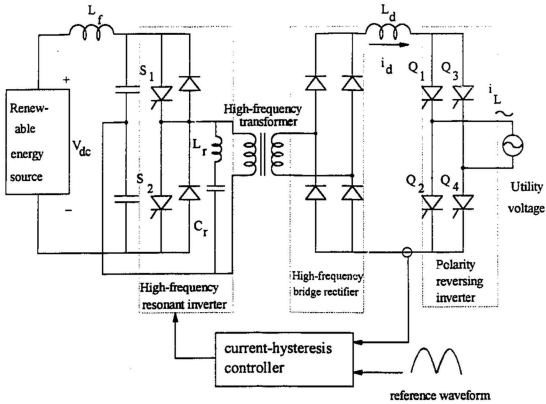


Figure 1.16: The High-frequency resonant link UIS.

not compatible with weak AC systems. Weak AC systems pose challenging problem from the point of view of maintaining stability and providing high-quality utility line current under varying conditions.

The current status of inverter control points to a wide variation in control strategies. Although the same inverter configuration may be used in UPS and UIS applications, the control strategies are very different. The variation is due to the fact that in the UPS, the load voltage is controlled so as to produce a sinusoidal voltage, whereas in the UIS the utility line current is the variable that is required to be sinusoidal.

The challenge is to find a control scheme that is applicable to both applications.

1.3 Thesis Objectives and Outline

The major objective of this study is to develop a cost-effective and practical control strategy for the voltage-source PWM inverter with output filter for both UPS and UIS applications. Efforts are directed at developing a unified control scheme to meet the performance objectives (such as high-quality load voltage and utility line current, and stability over a wide variation in system parameters) in both applications while providing improvement in the overall size, weight, and cost of the systems. To this end, a current-regulated, voltage-controlled scheme for voltage-source inverters with a second-order filter is proposed. The proposed scheme is capable of providing nearly perfect sinusoidal load voltage for UPS and sinusoidal line current for UIS. In addition to the inherent advantages of the inner-current, outer-voltage feedback control concept, the proposed scheme is compatible with non-linear loads. In UIS applications, the scheme is capable of injecting the utility line current into the power grid at any desired power factor. It is also compatible with both weak and large AC network applications.

The approach taken to characterize the proposed scheme for the two applications will involve four stages. First, the single-phase UPS system will be used as a vehicle to develop the control strategy. Second, the feasibility of the scheme will be demonstrated for the three-phase UPS. Third, a single-phase UIS will be investigated, and finally, the scheme will be applied to the three-phase UIS. A linearized model based on small-signal perturbation technique will be derived for each system. Low-frequency models will be developed and used to describe the steady-state operating charac-

teristics of the systems. Transfer functions describing the relationships between the power circuit variables and the control signal will be developed and used to examine the incremental dynamics of each system. In addition to these theoretical studies, laboratory proto-types of the UPS and the single-phase UfS will be developed to verify the theoretical results and demonstrate the feasibility of the proposed scheme. The remaining chapters of the thesis are organized as follows.

In chapter Two, a general model of the single-phase UPS system is developed in terms of the input DC voltage, power circuit parameters and inverter switching functions. The resulting general model of the system is discontinuous. Through the use of Fourier series analysis, the discontinuous model is replaced by two time-continuous models; the low-frequency and high-frequency models. These models are used to design the filter parameters. A small-signal linear dynamic model is then derived from the low-frequency model using the perturbation technique and small-signal approximation. The small-signal model of the system is used to study the power circuit incremental dynamics. Using root-locus technique, appropriate feedback variables that result in stable closed-loop operation of the system are selected. Using Bode diagrams and time-domain error analysis, feedback loop regulators of the inner current and the outer voltage loops are selected. Computer simulation results of the proposed UPS along with experimental verification for both linear and non-linear loads are presented.

Chapter Three extends the proposed control scheme to the three-phase UPS system taking into account the DC input filter dynamics. In order to cope with the time-varying system matrix of the general model, the forward-backward transformation is employed to transform the system state variables to the rotating frame of

reference where AC variables appear as DC quantities. The incremental dynamics of the power circuit state variables are then investigated to determine the stability of the system. It is shown that the proposed control scheme results in stable operation of the three-phase system over a wide range of parameter variation. Experimental results of the three-phase laboratory prototype of the system are provided to verify the computer simulation results and theoretical results obtained from the developed model.

The single-phase UIS with the proposed scheme is described in Chapter Four. Following the analytical techniques and procedures outlined in chapter two, the feasibility of the proposed scheme for UIS applications is investigated. The incremental dynamics of the power circuit variables are studied using the root-locus method. The results clearly show that directly using the utility line current as the only feedback variable leads to unstable operation of the UIS. On the other hand, the proposed scheme provides an indirect but stable control of the UIS. Experimental verification and computer simulation of the single-phase UIS model is presented along with its computer simulation.

Chapter Five deals with modeling, analysis, and design of the three-phase UIS system with input filter dynamics taken into account. The effect of various modes of operation of the UIS (e.g., unity power factor and zero-leading power factor operation) on the system dynamics is also investigated in the chapter. Computer simulation results of various waveforms of the three-phase UIS are presented.

Finally, in Chapter Six, a summary of the thesis highlighting the contribution of the research and suggestions for further work are outlined.

Chapter 2

The Single-Phase Voltage-Source Uninterruptible Power Supply System

This chapter deals with a novel real-time multiple feedback loop control strategy for single-phase voltage-source UPS systems. At the outset, a general analytical model is developed. Due to the switching nature of the power inverter, the system general model is discontinuous. Using Fourier series analysis, the discontinuous model is replaced by two time-continuous models; the low-frequency and the high-frequency models. These models are then employed to select optimum filter parameters.

A linearized small-signal model is derived, using perturbation and small-signal approximation, to describe the dynamic behavior of the system. This model is used to examine the incremental dynamics of the power circuit in order to select appropriate feedback variables which would result in stable operation of the closed-loop UPS system. To ensure both stable and high-quality load voltage, a real-time feedback control system configuration with an inner current and an outer voltage feedback loops is proposed for the operation of the single-phase voltage-source UPS system. Frequency-domain analysis of the proposed UPS system is carried out using Bode dia-

grams in order to select the appropriate control-loop regulators in both the inner and outer loops. Computer simulation results of a single-phase voltage-source half-bridge UPS inverter with a second-order filter and R-L load are presented to demonstrate the performance of the proposed control scheme. Experimental verification of a laboratory model of the UPS system is presented for both linear and non-linear loads so as to verify the predicted performance of the system.

2.1 General Model of the Single-Phase UPS Inverter

Figure 2.1 shows the power circuit of the single-phase voltage-source UPS system with R-L load. It consists of a half-bridge voltage-source inverter, an isolation transformer, a second-order $L_f - C_f$ filter and an $r_l - l_l$ load. The differential equations describing the behavior of the system variables are given by:

$$L_f \frac{di_i}{dt} = v_i - R_f i_i - v_c, \quad (2.1)$$

$$l_l \frac{di_l}{dt} = v_c - r_l i_l, \quad (2.2)$$

$$C_f \frac{dv_c}{dt} = i_c = i_i - i_l. \quad (2.3)$$

The voltage v_i in Eq. 2.1 is a function of the states of the power switches S_1 and S'_1 . For example, when switch S_1 is ON (i.e. S'_1 is OFF), $v_i = v_{dc}$. On the other hand, when S_1 is OFF (i.e. S'_1 is ON), $v_i = -v_{dc}$. Thus, expressing the voltage v_i in terms of the states of the power switches, Eq. (2.1) can be rewritten as,

$$L_f \frac{di_i}{dt} = (S_1^* - S'_1) v_{dc} - R_f i_i - v_c \quad (2.4)$$

where, $S_1^* = 1$ ($S'_1 = 0$) when S_1 is ON (S'_1 is OFF), $S_1^* = 0$ ($S'_1 = 1$) when S_1 is OFF (S'_1 is ON). Since either S_1 or S'_1 can be ON at any instant in time, the states

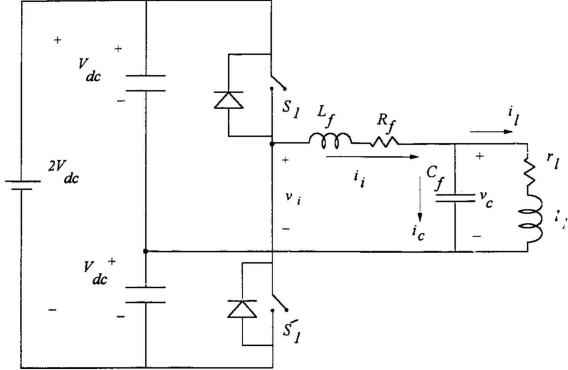


Figure 2.1: Single-phase voltage-source UPS inverter with R-L loads

of the power switches are governed by the identity

$$S_1^* + S_1^{*'} = 1. \quad (2.5)$$

Substituting Eq. (2.5) into Eq. (2.4), the system equations can be written in state-space representation as

$$\begin{bmatrix} \frac{di_i}{dt} \\ \frac{di_l}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & -\frac{r_l}{l_l} & \frac{1}{l_l} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_i \\ i_l \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} \\ 0 \\ 0 \end{bmatrix} (2S_1^* - 1)v_{dc}, \quad (2.6)$$

or

$$\dot{\mathbf{x}} = \mathbf{A} \mathbf{x} + \mathbf{B} \mathbf{e}^*. \quad (2.7)$$

Equation (2.6) was obtained without placing any restrictions on the inverter switching functions. Thus, the name “general” model is adopted.

Although Eq. (2.6) fully describes the system behavior during any ON/OFF period, it is time-discontinuous due to the presence of the discrete function S_1^* . Numerical analysis and computer simulation can be used to obtain the exact waveshapes of the system state variables, and to study the steady-state and dynamic performance of the system. However, this approach leads to trial-and-error procedures for designing the system. On the other hand, analytical models of the system can be obtained once the discrete function S_1^* is replaced with its time-continuous counterpart.

2.2 Time-Continuous Models of the UPS System

Two time-continuous analytical models of the UPS system are developed in this section. First, a low-frequency model is derived and used to study the system behavior at frequencies which are lower than the inverter switching frequency. A small-signal dynamic model is derived from the low-frequency model and used to examine the dynamic behaviour and design feedback regulators for closed loop operation of the system.

The high-frequency model, on the other hand, provides information about the system behavior at frequencies equal to or higher than the inverter switching frequency. This model, along with the low-frequency model, is used to determine the peak values of the inverter output current and capacitor current and voltage, and to select the appropriate filter parameters.

The sine pulse-width modulation scheme employed to generate the inverter switching pattern is periodic. Hence, assuming ideal inverter switching devices and neglect-

ing the dwell time when commuting from the upper to lower switching devices, the inverter output frequency spectrum can be determined using Fourier series analysis [101]. The switching function S_1^* can be represented by its Fourier series components as

$$S_1^*(t) = a_0 + \sum_{n=1}^{n=\infty} a_n \sin(n\omega_s t) + \sum_{n=1,3,5,\dots}^{n=\infty} b_n \cos(n\omega_s t), \quad (2.8)$$

where ω_s is the angular frequency of the inverter switching frequency. The Fourier series coefficients a_0 , a_n , and b_n are given by [102],

$$a_0 = d_1, \quad (2.9)$$

$$a_n = 0, \quad (2.10)$$

$$b_n = (-1)^n \frac{2}{n\pi} \sin(n\pi d_1). \quad (2.11)$$

where d_1 is the time average or the duty cycle of the switching function S_1^* . Replacing S_1^* in Eq. (2.6) by its Fourier components, Eq. (2.8), the system state-space equations can be rewritten as

$$\begin{aligned} \begin{bmatrix} \frac{di_i}{dt} \\ \frac{di_l}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} &= \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & -\frac{r_l}{L_l} & \frac{1}{L_l} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_i \\ i_l \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} \\ 0 \\ 0 \end{bmatrix} (2d_1 - 1) \\ &+ (-1)^n \sum_{n=1,3,5,\dots}^{\infty} \frac{4}{n\pi} \sin(n\pi \frac{d_1+1}{2}) \cos(n\omega_s t) v_{dc}. \end{aligned} \quad (2.12)$$

Upon examination of Eq. (2.12), it can be seen that the system forcing function is composed of the low-frequency driving function, $(2d_1 - 1)v_{dc}$, and the sum of high-frequency sinusoidal forcing functions, $(-1)^n \sum_{n=1,3,5,\dots}^{\infty} \frac{4}{n\pi} \sin(n\pi \frac{d_1+1}{2}) \cos(n\omega_s t) v_{dc}$. Consequently, Eq. (2.12) can be decomposed into low-frequency and high-frequency components. The system state-space equation can be rewritten in terms of low-frequency and high-frequency variables as

$$\dot{\mathbf{x}}_l + \mathbf{x}_h = \mathbf{A}(\mathbf{x}_l + \mathbf{x}_h) + \mathbf{B}(u_l + u_h), \quad (2.13)$$

where the subscript l and h denote the low-frequency and high-frequency components, and

$$u_l = (2d_1 - 1)v_{dc} \quad (2.14)$$

$$u_h = (-1)^n \sum_{n=1,3,5,\dots}^{\infty} \frac{4}{n\pi} \sin(n\pi \frac{d_1+1}{2}) \cos(n\omega_s t) v_{dc}. \quad (2.15)$$

2.2.1 The Low-Frequency Model

The low-frequency state-space equations are obtained from Eq. (2.12) as

$$\begin{bmatrix} \frac{di_l}{dt} \\ \frac{di_l}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_l}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & -\frac{r_l}{l_l} & \frac{1}{l_l} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_l \\ i_l \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{2d_1-1}{L_f} \\ 0 \\ 0 \end{bmatrix} v_{dc}. \quad (2.16)$$

For a modulating signal of the form,

$$v_m(t) = V_m \cos(\omega_m t), \quad (2.17)$$

the duty cycle, d_1 , is given by [102]

$$d_1 = \frac{1}{2}(m(t) + 1), \quad (2.18)$$

$$m(t) = \frac{V_m}{V_t} \cos(\omega_m t) = M \cos(\omega_m t), \quad (2.19)$$

where

$m(t)$ is the normalized modulating signal,

M is the modulation index ($= \frac{V_m}{V_t}$),

V_t is the amplitude of the carrier signal, and

ω_m is the angular frequency of the modulating signal.

Substituting Eq. (2.18) into Eq. (2.16), the system equations can be rewritten as

$$\begin{bmatrix} \frac{di_l}{dt} \\ \frac{di_l}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_l}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & -\frac{r_l}{l_l} & \frac{1}{l_l} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_l \\ i_l \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{m(t)}{L_f} \\ 0 \\ 0 \end{bmatrix} v_{dc} \quad (2.20)$$

Equation (2.20) shows that the forcing function of the UPS system at low frequencies is a function of the modulating signal and the input DC voltage.

2.2.2 Steady-State Analysis of the Low-Frequency Model

The steady-state model of the UPS circuit at frequencies lower than the inverter switching frequency is derived from Eq. (2.20) assuming that the resistance associated with the filter inductor is negligibly small, and all disturbances to the UPS system are absent. Figure 2.2 shows the steady-state equivalent circuit.

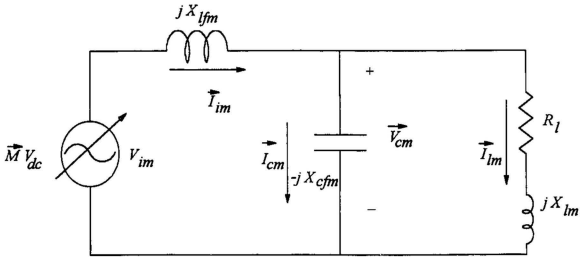


Figure 2.2: Circuit diagram of the steady-state low-frequency model

The steady-state variables \vec{I}_{im} , \vec{V}_{cm} , \vec{I}_{cm} , and \vec{I}_{lm} are obtained from Fig. 2.2 using phasor analysis as

$$\vec{I}_{im} = \frac{\vec{M} V_{dc}}{Z_{im}}, \quad (2.21)$$

$$\vec{V}_{cm} = \frac{\vec{M} V_{dc} (\cos \theta + j \sin \theta)}{(1 - H_{cm}) \cos \theta + j (X_{lfm} + (1 - H_{cm}) \sin \theta)}, \quad (2.22)$$

$$\vec{I}_{cm} = \frac{j \vec{V}_{cm}}{X_{cfm}}, \quad (2.23)$$

$$\vec{I}_{lm} = \frac{\vec{V}_{cm}}{\vec{Z}_{lm}} = \frac{\vec{V}_{cm}}{R_l + j X_{lm}}, \quad (2.24)$$

$$\vec{Z}_{im} = \frac{X_{cfm} (R_l (1 - H_{cm}) + j (X_{lfm} + (1 - H_{cm}) X_{lm}))}{X_{cfm} - X_{lm} + j R_l}, \quad (2.25)$$

where

$$H_{cm} = \omega_m^2 L_f C_f, \quad (2.26)$$

and Z_{lm} , Z_{im} , and θ are the load impedance, input impedance of the loaded filter, and the load angle respectively calculated at the angular frequency of the modulating signal. The subscript m indicates variables and parameters calculated at the frequency of the modulating signal.

2.2.3 The High-Frequency Model

The high-frequency state-space model of the UPS system is obtained from Eq. (2.12) as

$$\begin{aligned} \begin{bmatrix} \frac{di_i}{dt} \\ \frac{di_l}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} &= \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & \frac{r_l}{l_l} & \frac{1}{l_l} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_i \\ i_l \\ v_c \end{bmatrix} \\ &+ \begin{bmatrix} \frac{1}{L_f} \\ 0 \\ 0 \end{bmatrix} (-1)^n \sum_{n=1}^{\infty} \frac{4 V_{dc}}{n \pi} \sin(n \pi \frac{m(t)+1}{2}) \cos(n \omega_s t) \end{aligned} \quad (2.27)$$

Equation (2.27) shows that at frequencies equal to or higher than the switching frequency, the system forcing function is the sum of infinite number of sinusoidal voltages whose magnitude is dependent on the modulating signal, the input DC voltage and the order of the dominant harmonic. Substituting the value of $m(t)$ given by Eq. (2.19) into Eq. (2.27), the n^{th} harmonic component of the inverter output voltage

is given by

$$v_{in} = (-1)^n \sum_{n=1}^{\infty} \frac{4 V_{dc}}{n \pi} \sin(n \pi \frac{M \cos(\omega_m t) + 1}{2}) \cos(n \omega_s t) \quad (2.28)$$

Equation 2.28 shows that the high-frequency components in the inverter output voltage are amplitude modulated and have maximum values of $\frac{4V_{dc}}{n\pi}$ at $\omega t = \frac{\pi}{2}$. Figure 2.3 shows the waveshape of the dominant harmonic component. It is worth mentioning that as opposed to the hysteresis-band controllers [85, 86] or the Delta modulators [44, 48], where the frequency spectrum of the inverter switching pattern is both frequency and amplitude modulated, the frequency spectrum of the fixed-frequency sine pulse-width modulated inverter output is amplitude modulated. Thus, the design of an EMI filter that effectively prevents interference with equipments external to the power circuit can be easily carried out.

2.3 Selection of Filter Parameters

The goal of this section is to provide a graphical approach based on the low-frequency and high-frequency models to determine the values of L_f and C_f of the system filter that would result in small filter size, low cost, and load voltage total harmonic distortion less than 5%.

The selection of the filter parameters is carried out by first normalizing the circuit parameters. The following normalization of the circuit parameters is used:

1. the load impedance at the frequency of the modulating signal is assumed to be one per unit (pu),
2. all impedances and reactances are expressed as per unit of the load,

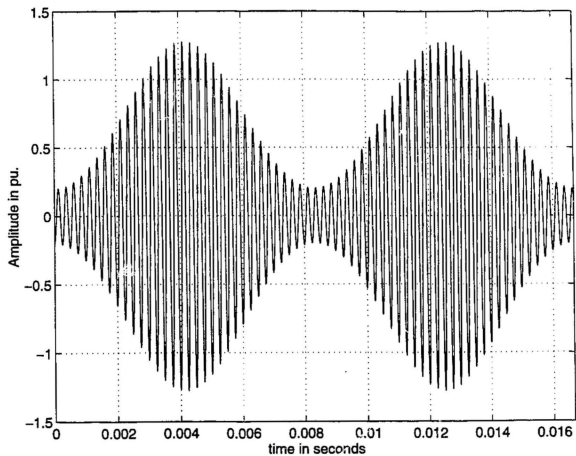


Figure 2.3: Waveshape of the dominant harmonic component in the inverter output voltage

3. the steady-state value of the input DC voltage, V_{dc} , is chosen as the base voltage and is equal to one pu,
4. all voltages are expressed as pu of V_{dc} .

It is assumed that the inverter output switching pattern is ideal, and the load power factor varies from 0.7 lagging to unity. The normalized n^{th} harmonic component of the inverter output voltage, v_{inp} , is obtained from Eq. (2.28) by substituting $V_{dc}=1$, and is given by

$$v_{inp} = \sum_{n=1}^{\infty} \frac{4}{n\pi} \sin\left(\frac{n\pi}{2}\right) \cos(n\omega_s t), \quad (2.29)$$

The size and cost of the filter are commensurate with its ratings. The filter ratings are determined for the worst-case condition of lagging power factor loads (0.7 pf lagging) [46]. Expressing the filter input impedance given by Eq. (2.25) in terms of the load impedance and load angle yields

$$\vec{Z}_{im} = \frac{|Z_{lm}| X_{cfm} ((1 - H_{cm}) \cos \theta + j (\frac{X_{lfm}}{|Z_{lm}|} + (1 - H_c) \sin \theta))}{|Z_{lm}| (\frac{X_{cfm}}{|Z_{lm}|} - \sin \theta + j \cos \theta)}. \quad (2.30)$$

The normalized input impedance of the loaded filter is obtained from Eq. (2.30) as

$$\vec{Z}_{imp} = \frac{X_{cfmp} ((1 - H_{cm}) \cos \theta + j (X_{lfmp} + (1 - H_{cm}) \sin \theta))}{X_{cfmp} - \sin \theta + j \cos \theta}, \quad (2.31)$$

where the *subscript p* denotes per unit values.

The normalized fundamental component of the inverter output current is given by

$$\vec{I}_{imp} = \frac{\vec{M}}{\vec{Z}_{imp}}, \quad (2.32)$$

and the normalized fundamental component of the capacitor (load) voltage is obtained from Eq. (2.22) as

$$\vec{V}_{imp} = \frac{\vec{M} (\cos \theta + j \sin \theta)}{(1 - H_{cm}) \cos \theta + j (X_{lfmp} + (1 - H_{cm}) \sin \theta)}. \quad (2.33)$$

The n^{th} harmonic component of the state variable of the loaded filter is determined for the worst-case scenario; i.e., when the dominant harmonic of the inverter output voltage is maximum.

The inverter input impedance at the n^{th} harmonic component is obtained as

$$\bar{Z}_{inp} = \frac{X_{cfs} ((1 - n^2 H_{cs}) \cos \theta + j n (X_{lfs} + (1 - n^2 H_{cs}) \sin \theta)}{X_{cfs} - n^2 \sin \theta + j n \cos \theta}, \quad (2.34)$$

where

$$X_{cfs} = \frac{\omega_m X_{cfsmp}}{\omega_s}, \quad (2.35)$$

$$X_{lfs} = \frac{\omega_s X_{lfsmp}}{\omega_m}, \quad (2.36)$$

$$H_{cs} = \frac{\omega_s^2 L_f C_f}{|Z_{lm}|^2}. \quad (2.37)$$

The corresponding filter input current is given by

$$\bar{I}_{inp} = \frac{\bar{V}_{inp}}{\bar{Z}_{inp}}. \quad (2.38)$$

The n^{th} harmonic component of the load voltage is obtained as

$$\bar{v}_{cnp} = \frac{\bar{V}_{inp} (\cos \theta + j n \sin \theta)}{(1 - n^2 H_{cs}) \cos \theta + j n (X_{lfs} + (1 - n^2 H_{cs}) \sin \theta)}. \quad (2.39)$$

The normalized volt-ampere reactive (VAR) rating of the filter series inductor is given by

$$Q_{lf} = \left(\frac{\hat{I}_{lmp}}{\sqrt{2}}\right)^2 X_{lfsmp} + \sum_{n=1}^{\infty} \left(\frac{\hat{I}_{inp}}{\sqrt{2}}\right)^2 n X_{lfs}. \quad (2.40)$$

The VAR rating of the filter shunt capacitor is given by

$$Q_{cf} = \left(\frac{\hat{V}_{cnp}}{\sqrt{2}}\right)^2 \frac{1}{X_{cfsmp}} + \sum_{n=1}^{\infty} \left(\frac{\hat{V}_{cnp}}{\sqrt{2}}\right)^2 \frac{n}{X_{cfs}}. \quad (2.41)$$

Another criteria that must be met is the total harmonic distortion (THD) of the load voltage. The lower the value of the THD of the load voltage the closer the load

voltage waveform is to a sinusoidal waveform and vice versa. The THD of the load voltage is defined by

$$THD\% = \frac{100}{V_{imp}} \sqrt{\sum_{n=2}^{\infty} V_{inp}^2}. \quad (2.42)$$

One more consideration for selecting the filter parameters is the attenuation of the fundamental component of the inverter output voltage. Better utilization of the input DC voltage is achieved if the voltage drop across the filter series inductor is kept at low values. The voltage attenuation is given by

$$\% \text{ Atten} = \frac{|\vec{V}_{imp}| - |\vec{V}_{lmp}|}{|\vec{V}_{lmp}|} \times 100. \quad (2.43)$$

In most UPS applications, systems of compact size are desirable. Since the load filter size contributes to the overall size of the system, a load filter with small size, and hence low ratings are desirable. Figure 2.4 shows the relationships between the filter parameters and the normalized filter ratings (NFR), attenuation of the fundamental component of the inverter output voltage, and the total harmonic distortion of the load voltage. Figure 2.4.a shows that the NFR of the filter inductor exhibits a minimum in the vicinity of $X_{lfm}=0.25$ pu for X_{cfm} less than or equal to 2.5 pu. Figure 2.4.b shows that the NFR of the filter capacitor monotonically decreases with increasing values of X_{cfm} and/or X_{lfm} . Figure 2.4.c shows that increasing the value of filter series inductor results in appreciable attenuation of the fundamental component of the inverter output voltage. Effective utilization of the input DC voltage is achieved if the attenuation is kept in the vicinity of 5%.

From Fig. 2.4.a, 2.4.b, and 2.4.c, the following filter parameters were chosen and considered optimum: $X_{lmp}=0.18$ pu and $X_{cfm}=2.5$ pu. These filter parameters result in 5.9% attenuation in the fundamental component of the inverter output volt-

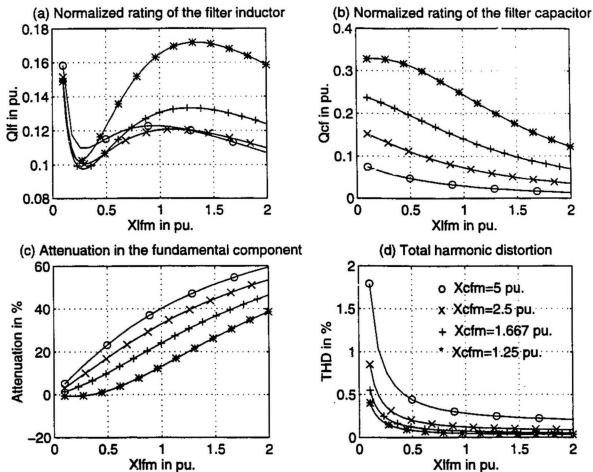


Figure 2.4: Effect of filter parameters on the normalized filter ratings, attenuation, and THD of the load voltage

age, an NFR of the filter inductor and capacitor of 0.1 pu and 0.14 pu. respectively, and load voltage THD of 0.5 %.

2.4 Small-Signal Dynamic Model

In order to ensure that the UPS will produce the nominal load voltage irrespective of disturbances such as variations and uncertainties in the input supply voltage, perturbations in the switching times, and disturbances in the load, a current-regulated feedback control scheme is proposed. In general, feedback control schemes are well-suited for UPS applications because of their high accuracy, fast dynamic response, and effectiveness in reducing the sensitivity of the output to parameter changes [103].

The objective of this section is to develop a small-signal model which describes the dynamic behavior of the system when perturbed from its nominal operating point. This model will be used to examine the stability of the UPS system under closed-loop control operation. The outcome of the stability study will determine the appropriate feedback variables which would result in successful operation of the feedback control of the UPS system. Also, the model will be used to conduct frequency-response analysis of the UPS system using Bode plots, the results of which will lead to the design of the control-loop regulators.

Although the system equations given by Eq. (2.20) are time-continuous, they are non-linear. The non-linearity arises from the variation in the load parameters, the DC voltage, and the modulating signal which are reflected in the cross product $\frac{v_c}{i_l}(t)$, $\frac{v_o(t)}{i_l}$, and $m(t) v_{dc}(t)$. In order to develop a dynamic model of the UPS system, the system equations are first linearized around a nominal steady-state operating point. This is carried out using the perturbation technique and small-signal approximation.

Using upper case letters to denote the steady-state variables, and assuming small deviations from the nominal values, the state variables of the system can be expressed as

$$\mathbf{x}(t) = \mathbf{X}(t) + \tilde{\mathbf{x}}(t); \quad (2.44)$$

i.e.,

$$i_i(t) = I_i(t) + \tilde{i}_i(t), \quad (2.45)$$

$$i_l(t) = I_l(t) + \tilde{i}_l(t), \quad (2.46)$$

$$v_c(t) = V_c(t) + \tilde{v}_c(t). \quad (2.47)$$

For the load,

$$r_l = R_l + \tilde{r}_l, \quad (2.48)$$

$$l_l = L_l + \tilde{l}_l. \quad (2.49)$$

For the control signal,

$$m(t) = M(t) + \tilde{m}(t); \quad (2.50)$$

and for the input voltage,

$$v_{dc}(t) = V_{dc} + \tilde{v}_{dc}(t). \quad (2.51)$$

Substituting Eqs. (2.45) to (2.51) into (2.20), results in

$$\begin{aligned} \frac{d}{dt} \begin{bmatrix} I_i(t) + \tilde{i}_i(t) \\ I_l(t) + \tilde{i}_l(t) \\ V_c(t) + \tilde{v}_c(t) \end{bmatrix} &= \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & -\frac{R_d + \tilde{r}_l}{L_l + \tilde{l}_l} & \frac{1}{L_l + \tilde{l}_l} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} I_i + \tilde{i}_i(t) \\ I_l + \tilde{i}_l(t) \\ V_c + \tilde{v}_c(t) \end{bmatrix} \\ &+ \begin{bmatrix} \frac{(I_i + \tilde{i}_i(t) + \tilde{m}(t))(V_{dc} + \tilde{v}_{dc}(t))}{L_f} \\ 0 \\ 0 \end{bmatrix}. \end{aligned} \quad (2.52)$$

Equation (2.52) can be reduced by assuming that the perturbations are sufficiently small such that higher-order terms and cross terms become negligibly small. For example, the element (2,2) of the system matrix in Eq. (2.52) can be written as

$$a_{22} = -\frac{R_l + \tilde{r}_l(t)}{L_l + \tilde{l}_l(t)} = -\frac{R_l}{L_l} \left(1 + \frac{\tilde{r}_l(t)}{R_l}\right) \left(1 + \frac{\tilde{l}_l(t)}{L_l}\right)^{-1}, \quad (2.53)$$

which can be approximated by

$$a_{22} \cong -\frac{R_l}{L_l} \left(1 + \frac{\tilde{r}_l(t)}{R_l} - \frac{\tilde{l}_l(t)}{L_l}\right). \quad (2.54)$$

Similarly, element (2,3) can be approximated by

$$a_{23} \cong \frac{1}{L_l} \left(1 - \frac{\tilde{l}_l(t)}{L_l}\right). \quad (2.55)$$

Substituting Eq. (2.54) and Eq. (2.55) into Eq. (2.52), and once more neglecting cross terms and higher-order terms, Eq. (2.52) can be approximated by

$$\begin{aligned} \frac{d}{dt} \begin{bmatrix} I_i(t) \\ I_l(t) \\ V_c(t) \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} \tilde{i}_i(t) \\ \tilde{i}_l(t) \\ \tilde{v}_c(t) \end{bmatrix} &\cong \begin{bmatrix} -\frac{R_l}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & -\frac{R_l}{L_l} & \frac{1}{L_l} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} I_i(t) \\ I_l(t) \\ V_c(t) \end{bmatrix} \\ &+ \begin{bmatrix} 0 & 0 & 0 \\ 0 & -\frac{R_l}{L_l} \left(\frac{\tilde{r}_l}{R_l} - \frac{\tilde{l}_l}{L_l}\right) & -\frac{\tilde{l}_l}{L_l^2} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_i(t) \\ I_l(t) \\ V_c(t) \end{bmatrix} \\ &+ \begin{bmatrix} -\frac{R_l}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & -\frac{R_l}{L_l} & \frac{1}{L_l} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_i(t) \\ \tilde{i}_l(t) \\ \tilde{v}_c(t) \end{bmatrix} \\ &+ \begin{bmatrix} \frac{\tilde{m}(t)V_{dc}}{L_f} + \frac{M(t)\tilde{v}_{dc}(t)}{L_f} + \frac{V_{dc}M(t)}{L_f} \\ 0 \\ 0 \end{bmatrix}. \end{aligned} \quad (2.56)$$

Since the nominal solution itself satisfies the system state equations, the system linearized model is obtained from Eq. (2.56) as

$$\frac{d}{dt} \begin{bmatrix} \tilde{i}_i(t) \\ \tilde{i}_l(t) \\ \tilde{v}_c(t) \end{bmatrix} \cong \begin{bmatrix} 0 & 0 & 0 \\ 0 & -\frac{1}{L_l} & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_i(t) \\ I_l(t) \\ V_c(t) \end{bmatrix} \tilde{r}_l$$

$$\begin{aligned}
& + \begin{bmatrix} 0 & 0 & 0 \\ 0 & \frac{R_l}{L_l} & -\frac{1}{L_l} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_i(t) \\ I_l(t) \\ V_c(t) \end{bmatrix} \tilde{l}_l \\
& + \begin{bmatrix} -\frac{R_l}{L_l} & 0 & -\frac{1}{L_l} \\ 0 & -\frac{R_l}{L_l} & \frac{1}{L_l} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_i(t) \\ \tilde{i}_l(t) \\ \tilde{v}_c(t) \end{bmatrix} \\
& + \begin{bmatrix} \frac{\tilde{m}(t) V_{dc}}{L_f} + \frac{M(t) \tilde{v}_{dc}(t)}{L_f} \\ 0 \\ 0 \end{bmatrix}. \tag{2.57}
\end{aligned}$$

Equation (2.57) is the linearized small-signal model of the single-phase UPS system. Various transfer functions of the system can be derived from the equation. For example, the transfer function of the incremental changes in the control signal, $\tilde{m}(s)$, to the incremental changes in any of the state variables can be obtained from Eq. (2.57) by setting the other small-signal variables (i.e., the load disturbance \tilde{r}_l , \tilde{l}_l , and input DC voltage variations \tilde{v}_{dc}) to zero and taking the Laplace transform of the resulting equation. Similarly, the transfer function that relates the variations in the input or output disturbances (e.g. the input DC voltage or load disturbances, \tilde{r}_l , \tilde{l}_l) to the system state variables can be obtained by setting the other disturbances to zero and taking Laplace transform of the resulting equation.

Although it is possible to obtain the transfer function for load variations, Eq. (2.57) shows that the process will involve obtaining the Laplace transform of the multiplication of two time-dependent variables, namely, $\tilde{r}_l I_l(t)$, $\tilde{l}_l I_l(t)$, and $\tilde{l}_l V_c(t)$, which translates into a convolution integral in the frequency domain. Since the perturbation can be any time-varying function, the resultant analytical expression becomes too complicated and intractable. Therefore, it is easier to investigate the effect of load variations on the system dynamics using numerical simulations.

The transfer function of the control to the state variables is obtained from Eq. (2.57) by substituting $\tilde{v}_{dc}(t) = \tilde{r}_l = \tilde{l}_l = 0$. The result is

$$\frac{d}{dt} \begin{bmatrix} \tilde{i}_i(t) \\ \tilde{i}_l(t) \\ \tilde{v}_c(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_l}{L_l} & 0 & -\frac{1}{L_l} \\ 0 & -\frac{R_l}{L_l} & \frac{1}{L_l} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_i(t) \\ \tilde{i}_l(t) \\ \tilde{v}_c(t) \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{L_l} \\ 0 \\ 0 \end{bmatrix} \tilde{m}(t). \quad (2.58)$$

Equation (2.58) can be expressed in the form

$$\dot{\tilde{\mathbf{x}}} = \mathbf{A} \tilde{\mathbf{x}} + \mathbf{B} \tilde{m}(t). \quad (2.59)$$

Taking the Laplace transform of Eq. (2.59), the transfer function of the incremental changes in the control signal for incremental changes in the system state variables is obtained as

$$\frac{\tilde{\mathbf{x}}(s)}{\tilde{m}(s)} = (s\mathbf{I} - \mathbf{A})^{-1} \begin{bmatrix} \frac{V_{dc}}{L_l} \\ 0 \\ 0 \end{bmatrix}, \quad (2.60)$$

where s is the Laplace operator, and \mathbf{I} is the identity matrix.

Equation (2.60) can be rewritten as

$$\frac{\begin{bmatrix} \tilde{i}_i(s) \\ \tilde{i}_l(s) \\ \tilde{v}_c(s) \end{bmatrix}}{\tilde{m}(s)} = \frac{\frac{V_{dc}}{L_l} \begin{bmatrix} s^2 + \frac{R_l}{L_l}s + \frac{1}{L_l C_f} \\ \frac{1}{C_f L_l} \\ \frac{1}{C_f} (s + \frac{R_l}{L_l}) \end{bmatrix}}{(s + \frac{R_l}{L_l})(s + \frac{R_l}{L_l}) + \frac{1}{C_f L_l} + \frac{1}{C_f L_l} (s + \frac{R_l}{L_l})}. \quad (2.61)$$

Equation (2.61) gives the transfer function of the system state variables due to incremental changes in the modulating signal.

2.5 Selection of Feedback Control Scheme

The objective of the control system of the UPS system is to produce a sinusoidal load voltage that closely follows a reference sinusoidal waveform with very low harmonic content. To do so, three possible variables, namely, the capacitor voltage, capacitor

current, and the inverter output current, can be employed to establish a feedback control algorithm. In order to select the appropriate feedback variable which results in stable operation of the UPS system under adverse operating conditions, the incremental dynamics of these variables due to incremental changes in the modulating signal are examined using the root-locus method. It is assumed that the incremental variation in the control signal is much slower than the bandwidth of the control loop. Hence, a quasi-static approach is used to carry out the investigation [87, 89, 104, 105].

2.5.1 Capacitor (Load) Voltage as Feedback Variable

The transfer function of the incremental changes in the capacitor (load) voltage due to incremental changes in the modulating (control) signal is obtained from the third row of Eq. (2.61) as

$$\frac{\tilde{v}_c(s)}{\tilde{m}(s)} = \frac{\frac{V_{dc}}{C_f} (s + \frac{R_L}{L_L})}{L_f (s^3 + (\frac{R_L}{L_L} + \frac{R_L}{L_f}) s^2 + (\frac{1}{C_f L_L} + \frac{R_f R_L}{L_f L_L} + \frac{1}{C_f L_f}) s + \frac{R_f + R_L}{C_f L_f L_L})}. \quad (2.62)$$

Figure 2.5 shows the root locus of the incremental dependence of the capacitor voltage due to incremental changes in the modulating signal for various loading conditions and the following system parameters:

$$Z_L = 10 \Omega, \quad V_{dc} = 100.0 \text{ Volts}, \quad L_f = 5.0 \text{ mH}, \text{ and } C_f = 100.0 \mu\text{F}.$$

The Figure shows that a simple closed-loop control involving the capacitor voltage as the only feedback variable would make two of the system poles move along the imaginary axis of the s-plane. This has the effect of producing high-frequency oscillations in the load voltage for wide variation in the load conditions. For the chosen circuit parameters, the figure shows that the frequency of oscillation could reach 4430.0 rad./sec for a 10% change in the modulating signal. However, in the case of unity

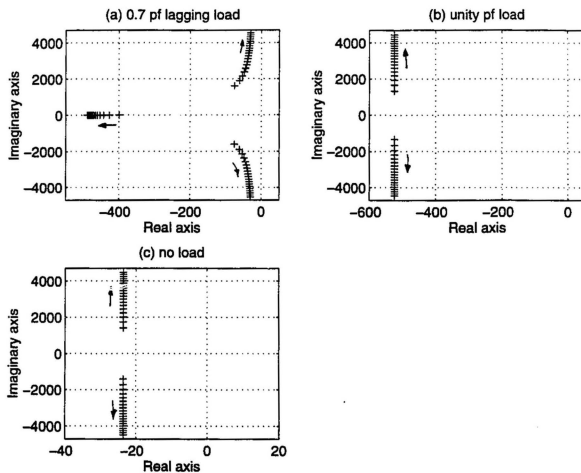


Figure 2.5: Root locus of the incremental dependence of the capacitor voltage due to incremental changes in the modulating signal at various loading conditions

power factor loads, the system oscillations have higher damping ratio since the system poles are shifted farther into the left-hand side of the s-plane. Figures 2.6 to 2.9 show simulation results of various waveforms in the single-phase voltage-source UPS with the capacitor voltage as the only feedback control variable for the following system parameters:

$$\begin{array}{lll} \text{switching frequency, } F_s=4.0 \text{ kHz,} & & \text{modulating signal, } M=0.9, \\ V_{dc}=100.0 \text{ Volts,} & L_f=5.0 \text{ mH,} & C_f=100.0 \text{ }\mu\text{F.} \end{array}$$

Figures 2.6 and 2.7 show the inverter output switching pattern, inverter output current, load (capacitor) voltage, and load current for 0.7 pf lagging load. Figure 2.7.a confirms that the capacitor voltage has a high-frequency oscillation superimposed on it. The maximum value of the frequency of oscillation as obtained from Fig. 2.7 is 4189.0 rad/sec.

Figures 2.8 and 2.9 show simulation results of the inverter output voltage, output current, load (capacitor) voltage, and load current for unity power factor loads. Figure 2.9.a shows that the load voltage has high-frequency oscillation but with a much faster rate of decay.

2.5.2 Inverter Output Current as Feedback Variable

The open-loop transfer function of the incremental changes of the modulating signal to the incremental changes in the inverter output current is obtained from Eq. 2.61 as

$$\frac{\tilde{i}_i(s)}{\tilde{m}(s)} = \frac{V_{dc} \left(s^2 + \frac{R_L}{L_L} s + \frac{1}{L_L C_f} \right)}{L_f \left(s^3 + \left(\frac{R_L}{L_L} + \frac{R_f}{L_f} \right) s^2 + \left(\frac{1}{C_f L_L} + \frac{R_f R_L}{L_f L_L} + \frac{1}{C_f L_f} \right) s + \frac{R_f + R_L}{C_f L_f L_L} \right)}. \quad (2.63)$$

Figure 2.10 shows the root locus of Eq. (2.63). The figure shows that simply closing the loop around the inverter output current makes the system poles move

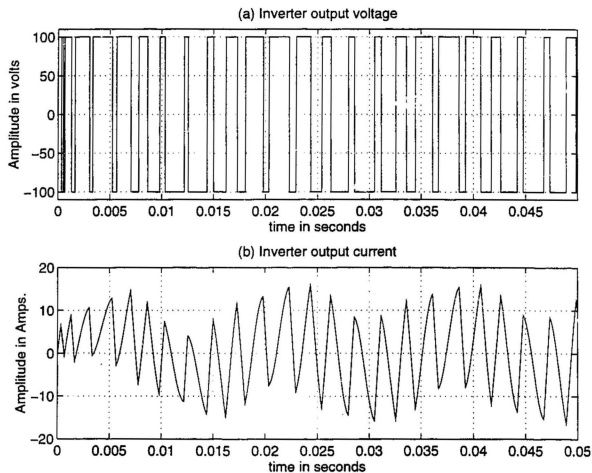


Figure 2.6: Computer simulation results of the inverter output voltage and current of the single-phase UPS system with 0.7 pf lagging load and the capacitor voltage employed as the feedback variable

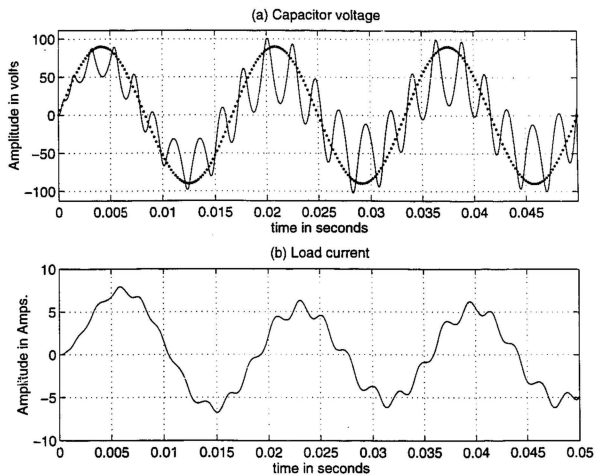


Figure 2.7: Computer simulation results of the load (capacitor) voltage and load current of the single-phase UPS system with 0.7 pf lagging load and the capacitor voltage employed as the feedback variable

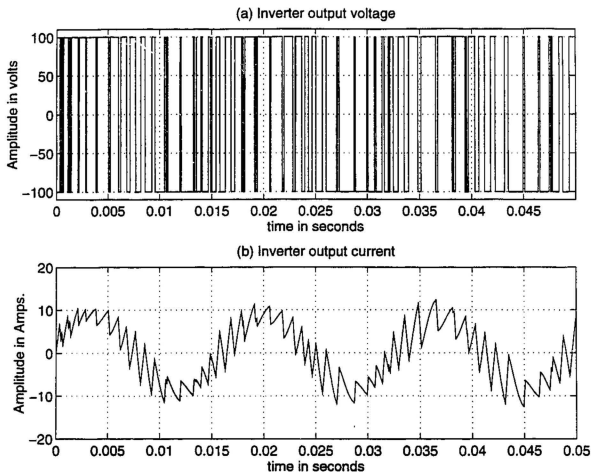


Figure 2.8: Computer simulation results of the inverter output voltage and current of the single-phase UPS system with unity power factor load and the capacitor voltage employed as the feedback variable

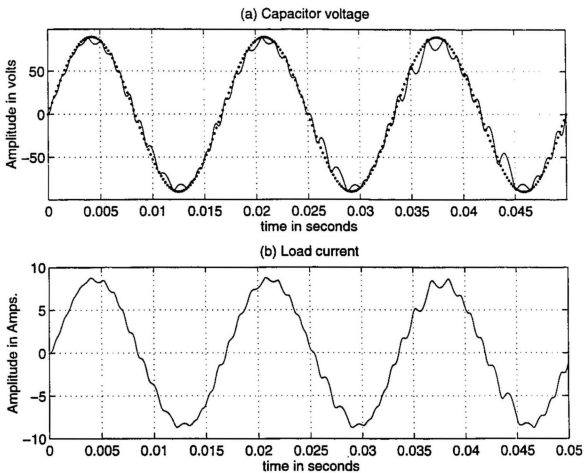


Figure 2.9: Computer simulation results of the load (capacitor) voltage and load current the of single-phase UPS system with unity power factor load and the capacitor voltage employed as the feedback variable

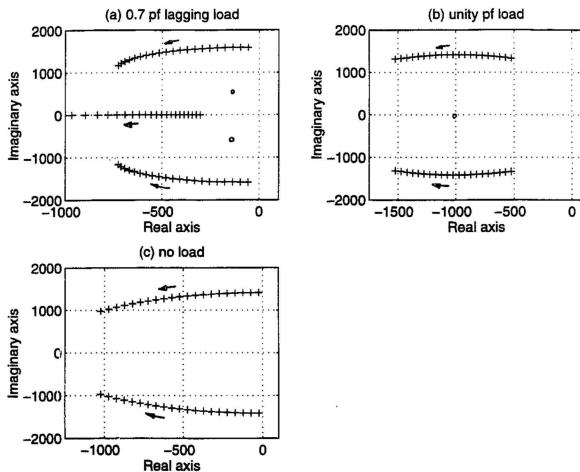


Figure 2.10: Root locus of the incremental dependence of the inverter output current due to incremental changes in the modulating signal

farther to the left of the left-hand side of the s-plane, resulting in stable closed-loop operation of the UPS system.

However, selecting the inverter output current as the feedback variable creates a current source out of the power inverter. The single-phase UPS system can, therefore, be modeled as a current source feeding current into the parallel circuit comprising the filter shunt capacitor, C_f , and the $R_l - L_l$ load as shown in Fig 2.11. The model

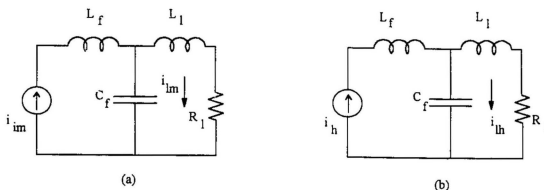


Figure 2.11: Circuit model of the single-phase UPS system with the inverter output current employed as the feedback variable: a) at the fundamental frequency of the modulating signal, b) at higher-order harmonics of the inverter output current

shows that the filter shunt capacitor along with the load circuit constitute a parallel resonance circuit which, depending on the value of L_l , could resonate at one of the frequency components of the inverter output current. This case is likely to occur when the load power factor is closer to unity. This is due to the fact that the resonant frequency of the tank circuit becomes closer to the inverter switching frequency.

In order to prevent resonance in the load circuit, an outer load (capacitor) voltage feedback loop can be incorporated to provide damping of any oscillations that may

occur in the load circuit. However, in order to generate the reference waveform of the inverter output current, the load current must be sensed [58]. Therefore, to successfully operate the UPS with inverter output current as the feedback variable, an extra current sensor is required, making the system costly. Consequently, selecting the inverter output current as the feedback variable is overruled.

2.5.3 Capacitor Current as the Feedback Variable

The incremental changes in the capacitor current is given by

$$\tilde{i}_c(s) = \tilde{i}_i(s) - \tilde{i}_l(s). \quad (2.64)$$

The open-loop transfer function relating the incremental changes in the capacitor voltage to incremental changes in the modulating signal is given by

$$G_{ic}(s) = \frac{\tilde{i}_c(s)}{\tilde{m}(s)} = \frac{V_{dc} s (s + \frac{R_L}{L_f})}{L_f (s^3 + (\frac{R_L}{L_f} + \frac{R_L}{L_f})s^2 + (\frac{1}{C_f L_f} + \frac{R_f R_L}{L_f L_f})s + \frac{R_f + R_L}{C_f L_f L_f})}. \quad (2.65)$$

The root locus of Eq. (2.65) is depicted in Fig. 2.12. The figure shows that closing the loop around the capacitor current moves the system poles farther to the left of the left-hand side of the s-plane. Thus, employing the capacitor current as the feedback variable of the single-phase voltage-source UPS inverter would result in stable operation of the overall closed-loop system.

Figure 2.13 shows the circuit diagram of the single-phase voltage-source UPS inverter employing the capacitor current as the only feedback variable in the control circuit. Although this control scheme would result in a sinusoidal capacitor current, it does not guarantee a sinusoidal capacitor voltage. Non-sinusoidal load voltages are likely to occur in PWM power supplies where the inverter output voltage is a chopped

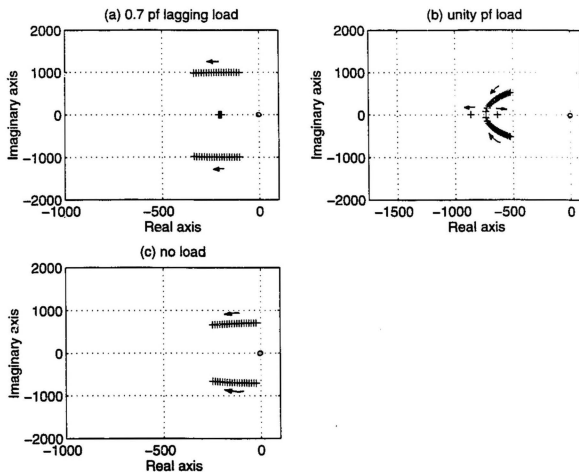


Figure 2.12: Root locus of the incremental dependence of the capacitor current due to incremental changes in the modulating signal

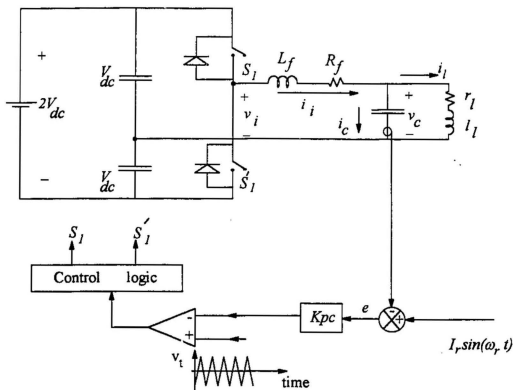


Figure 2.13: Control of the single-phase UPS system employing the capacitor current as the only feedback variable

DC voltage. Therefore, to ensure both sinusoidal capacitor voltage and current, an outer capacitor voltage feedback loop is incorporated.

2.5.4 The Proposed Control Scheme

For successful operation of the single-phase voltage-source UPS system, a control scheme which consists of an inner capacitor current loop and an outer capacitor voltage feedback loop is proposed. Figure 2.14 shows the proposed UPS system. The principle of operation is as follows. The actual capacitor voltage is sensed and

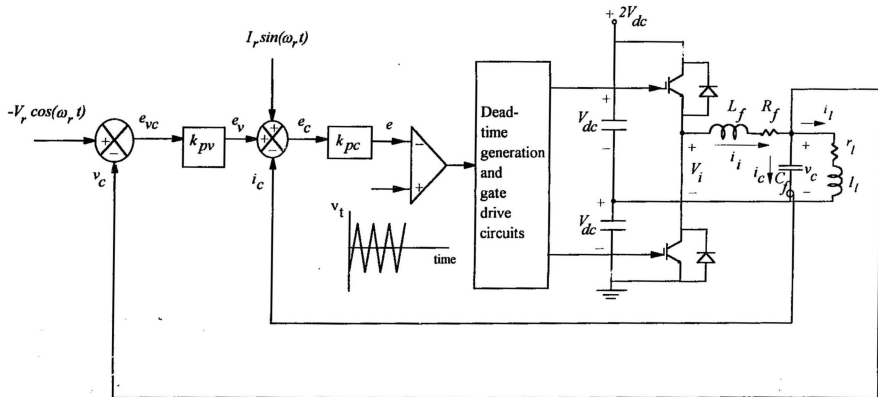


Figure 2.14: The proposed control strategy of the single-phase voltage-source UPS system

compared with its reference waveform, $-V_r \cos(\omega_r t)$, to produce the error voltage e_{vc} . e_{vc} is then passed through a proportional controller to produce the error signal e_v . The latter is summed with the difference between the actual capacitor current and its reference waveform, $I_r \sin(\omega_r t)$, to produce the error signal e_c . e_c is then conditioned via a proportional controller in the current loop to produce the error signal e . The latter is compared with a fixed-frequency triangular waveform in a hard limiter. The resulting switching pattern at the output of the hard limiter is used to control the inverter switching devices such that the error between the actual capacitor voltage and current waveforms and their respective reference waveforms is reduced.

The resultant control system configuration offers many advantages for UPS operation. The inner capacitor current loop provides an inherent peak current limit in the capacitor, which in effect acts to limit the high current surges at the inverter output especially during “cold” start of the system. In addition, since the capacitor current represents the rate of change of the load voltage, the control scheme is capable of predicting and correcting near future variations in the load voltage and thus providing fast dynamic response of the overall system. Furthermore, the outer voltage loop regulates the load voltage and ensures that the load voltage closely follows its reference sinusoidal waveform with minimum steady-state error and low total harmonic distortion.

The single-phase voltage-source UPS system shown in Fig. 2.14 is simulated to obtain various waveforms of the power circuit variables. Closed form solution of the power circuit state variables within a switching interval (ON/OFF) were obtained using symbolic computation package, MAPLE [106, 107]. The closed form solution and the control algorithm were employed to obtain the switching instants of the power

switching devices.

The following system parameters were used to obtain the waveforms of the various state variables of the UPS system shown in Fig. 2.14:

$$\begin{array}{llll} k_{pc}=1, & k_{pv}=1, & V_{dc}=100.0 \text{ Volts}, & L_f=5.0 \text{ mH}, & C_f=100.0 \mu\text{F}, \\ Z_l=10.0 \Omega, & \text{at } 0.7 \text{ pf lagging}, & & M=0.9, & F_s=4.0 \text{ kHz}. \end{array}$$

Figure 2.15 shows the inverter output voltage and current waveforms. The inverter output voltage waveform (Fig. 2.15.a) shows that the control scheme produces a pulse-width modulated switching pattern with constant switching frequency and variable duty cycle. The figure shows that the inverter output current (Fig. 2.15.b) is sinusoidal with superimposed high-frequency switching harmonics.

The capacitor voltage waveform (Fig. 2.16.a) exhibits a nearly perfect sinusoid. The steady-state error in the capacitor voltage and its reference waveform can be significantly reduced by properly adjusting the controller gain (as will be shown in Section 2.6).

The shunt capacitor current waveform (Fig. 2.16.b) shows that the instantaneous capacitor current is constrained to follow a reference sinusoidal waveshape. The constant frequency nature of the control scheme, however, results in a wider instantaneous current variation around the peak values of the reference waveform. The range of current excursions is determined by the controller gains, switching frequency, and the amplitude of the high-frequency carrier waveform.

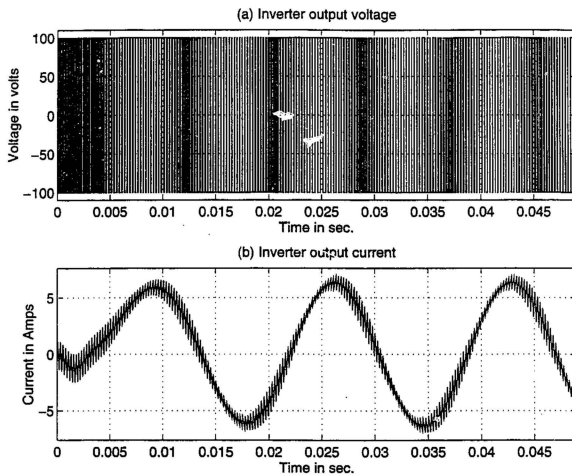


Figure 2.15: Computer simulation waveforms in the single-phase UPS system employing the proposed control scheme

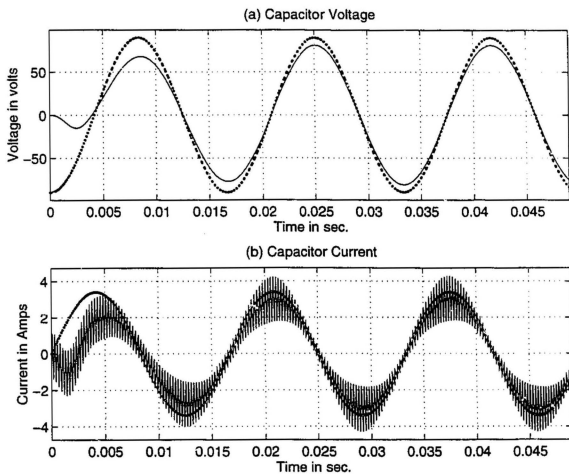


Figure 2.16: Computer simulation waveforms of the capacitor voltage and current in the single-phase UPS system employing the proposed control scheme

2.6 Frequency Domain Analysis and Design of the Proposed Scheme

In Section 2.5.4, it was shown that the proposed real-time feedback control scheme comprising the inner capacitor current and the outer load voltage feedback loops resulted in successful operation of the single-phase UPS system. However, in order to obtain a control scheme that has fast dynamic response and small steady-state error, both feedback loops (the inner and outer loops) should be carefully designed. The design of the feedback loops will be carried out in this section. The following approach is followed, with the outer voltage loop open, the frequency response of the inner current loop is first examined and a proper compensator is selected. Then, with the inner current loop closed, the frequency response of the outer voltage loop is examined and an appropriate compensator is selected.

2.6.1 Frequency Domain Analysis of the Inner Current Loop

The open-loop transfer function of the incremental variation in the modulating signal to incremental changes in the capacitor current is given by Eq. (2.65). Substituting the following system variables:

$$L_f = 5.0 \text{ mH}, \quad C_f = 100.0 \text{ } \mu\text{F}, \quad R_l = 6.65 \text{ } \Omega, \quad L_l = 15 \text{ mH}, \quad V_{dc} = 75.0 \text{ Volts},$$

in Eq. (2.65) results in

$$G_{ic}(s) = 1.5 \times 10^4 \frac{s(s + 406.25)}{s^3 + 453.40 s^2 + 264.4 \times 10^4 s + 842.00 \times 10^6}. \quad (2.66)$$

The denominator of Eq. (2.66) is the characteristic polynomial of $G_{ic}(s)$, and its roots yield the open-loop poles of the system. The system has a real negative pole at

$$p_1 = -323.56, \quad (2.67)$$

and a complex conjugate pole pair at

$$p_{2,3} = \sigma \pm j\omega = -64.91 \pm j1611.80. \quad (2.68)$$

The roots of the numerator of Equation (2.66) yield the system zeros and they are located at

$$z_1 = 0.0, \quad (2.69)$$

$$z_2 = -406.25. \quad (2.70)$$

It can be seen from Equations (2.67) and (2.70) that the real negative pole of $G_{ic}(s)$, p_1 , is located in close proximity to the real negative z_2 . Hence, this pole-zero arrangement cancel the effect of one another and the system order can be reduced by one. The reduced-order transfer function is given by

$$G_{icr}(s) = 1.88 \times 10^4 \frac{s}{(s + 64.91)^2 + 1611.80^2}, \quad (2.71)$$

where the subscript r denotes a reduced-order transfer function. The resulting second-order system has lightly-damped poles with damping ratio $\zeta = 0.04$.

Figure 2.17 shows the Bode plot of the transfer function of the inner current loop at various loading conditions. The figure shows that the inner current loop exhibits a band-pass filter-like characteristics. It can be seen that, irrespective of the load conditions, the magnitude of the capacitor current at very low frequencies is severely attenuated. This is due to the fact that the impedance of the capacitor is very high at low frequencies. Also, the magnitude of the current in the filter capacitor is attenuated at high frequencies. This is a result of the high impedance of filter series inductor at high frequencies, and hence the appreciable voltage drop across the filter series inductor. The figure also shows that the bandwidth of the inner current is not

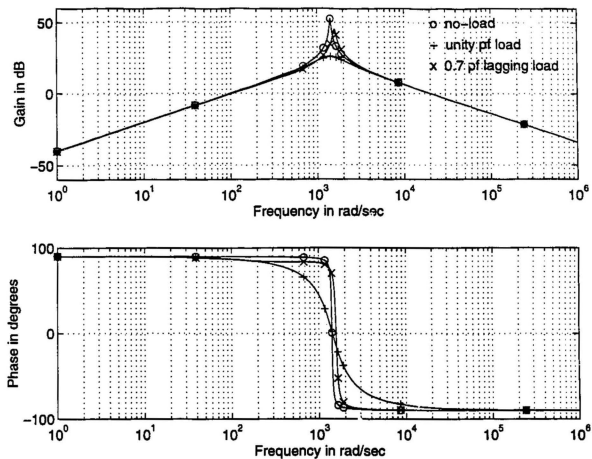


Figure 2.17: Bode plot of the open-loop transfer function of the inner current loop at various loading conditions

affected by the load variations. However, for unity power factor loads, the system exhibits lower resonant peak (23.68 dB) due to the higher damping ratio introduced by the load resistance.

2.6.2 Frequency Domain Design of the Inner Current Loop

Figure 2.17 shows that the open-loop transfer function of the inner current loop - irrespective of the system loading condition - crosses the zero dB line (unity gain) at a phase angle of $\pm 90.0^\circ$. This translates into a theoretical gain margin of infinity and phase margin of 270.0° and 90.0° . Thus, the inner capacitor current loop possesses good stability measures.

The closed-loop transfer function of the inner capacitor current loop for various loading conditions is shown in Figs. 2.18 to 2.20. The figures show that the inner current loop exhibits a near-unity gain over the range of 200.0 rad./sec ($\cong 32.0\text{ Hz}$) to 10,000 rad./sec. ($\cong 1600.0\text{ Hz}$) with the introduction of some phase error in the output signal. However, Fig. 2.19 shows that the loop gain is highest for 0.75 power factor lagging loads.

In order to avoid excessive gain of the inner current loop and produce a system that is immune to switching noise, the bandwidth of the the inner current loop should not be too wide. Hence, the design of the inner current loop will be carried out for worst-case condition of 0.75 power factor lagging loads.

The gain of the closed-loop transfer function of the inner current loop is designed to be nearly unity over the range of frequency of interest ($\omega \cong 200\text{ rad/sec}$ up to approximately half the inverter switching frequency). The gain can be increased by using a proportional controller (k_{pc}) in the feed-forward path of the inner current

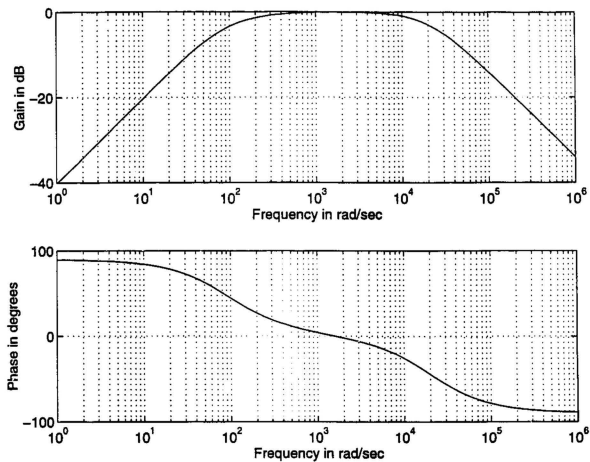


Figure 2.18: Closed-loop frequency response of the inner current loop with no-load

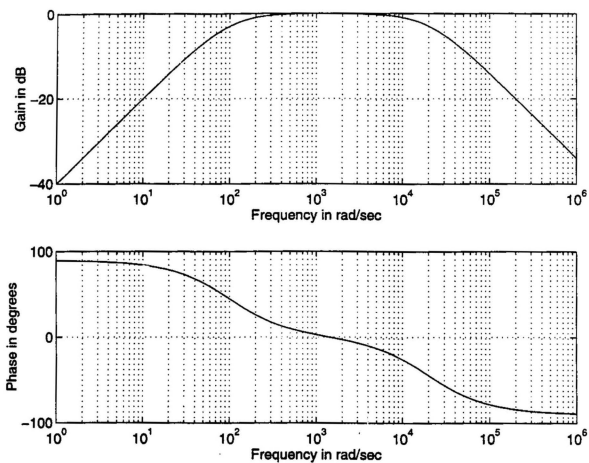


Figure 2.19: Closed-loop frequency response of the inner current loop with 0.75 pf lagging load

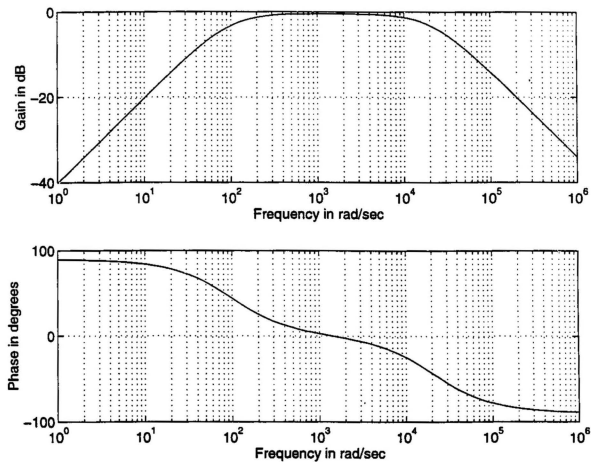


Figure 2.20: Closed-loop frequency response of the inner current loop with unity power factor load

loop. The higher the value of k_{pc} the closer the closed-loop gain will be to unity. On the other hand, very high values of k_{pc} would make the loop bandwidth too wide and causes the system to become susceptible to high-frequency switching noise. A proportional controller of value $k_{pc}=2.0$ is chosen. Figure 2.21 shows the closed-loop transfer function of the inner current with $k_{pc}=2.0$. The closed-loop gain at half the inverter switching frequency is 0.94.

2.6.3 Frequency Domain Analysis of the Outer Voltage Loop

The open-loop transfer function of the outer voltage loop is obtained in terms of the closed-loop transfer function of the inner current loop as

$$G_{ucr}(s) = \frac{1}{s C_f} \frac{k_{pc} G_{icr}}{1 + k_{pc} G_{icr}(s)}. \quad (2.72)$$

Substituting the value of G_{icr} and C_f into Eq. (2.72), it can be shown that the open-loop transfer function of the outer voltage loop has three negative real poles at -3.20×10^4 , -3.87×10^2 , -61.75 , and a negative real zero at -3.70×10^2 .

Figure 2.22 shows the Bode plot of the open loop transfer function of the outer voltage loop. The figure shows that the loop has a phase margin of 74.0° and a gain margin of 87.1 dB.

2.6.4 Frequency-Domain Design of the Outer Voltage Loop

The steady-state error between the capacitor voltage and its reference waveform should be kept very small. One way of achieving this is, once again, to use a proportional controller k_{pv} whose value is greater than unity. Figure 2.22 shows that a high value of the k_{pv} shifts the system crossover frequency to higher values, thus reducing the available gain and phase margin in the outer voltage loop.

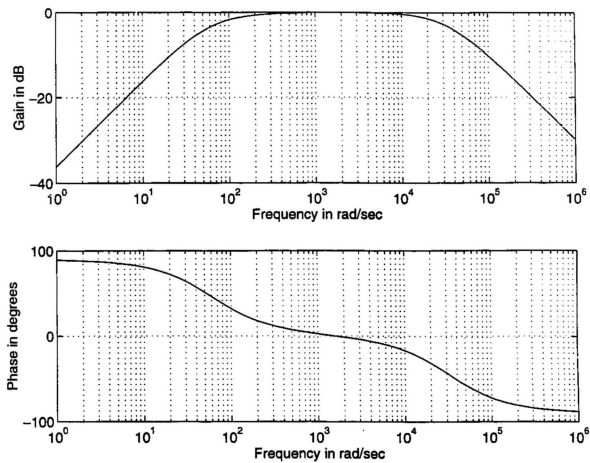


Figure 2.21: Closed-loop frequency response of the inner current loop for 0.75 power factor load and $k_{pc}=2.0$

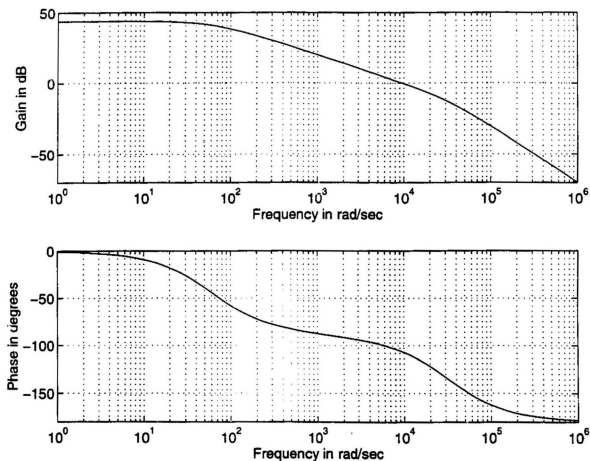


Figure 2.22: Bode plot of the open-loop transfer function of the outer voltage loop

Figure 2.23 shows the effect of k_{pv} on the steady state error between the capacitor voltage and its reference sinusoidal waveform. The error was computed by carrying out several computer runs for various values of k_{pv} with $k_{pc}=2.0$. The figure shows that the error decreases for increasing values of k_{pv} , and for $k_{pv} \geq 2.75$, the error is less than 2.0 %. Thus k_{pv} is chosen as 2.75.

2.7 Computer Simulation

The closed-loop operation of the proposed control strategy shown in Fig. 2.14 was simulated to obtain various waveforms in the UPS system. The following system parameters were used:

$$L_f = 5.0 \text{ mH}, \quad C_f = 100.0 \text{ } \mu\text{F}, \quad R_l = 6.5 \text{ } \Omega, \quad L_l = 15.0 \text{ mH}, \quad V_{dc} = 75.0 \text{ Volts.}$$

Figures 2.24 to 2.26 show the simulation results of various waveforms of the proposed UPS system with the selected values of the controller gains. Figure 2.25 show that the system requires only a quarter cycle (based on 60 Hz frequency) to bring the system from “cold” start to steady-state full-load operation. The figure also shows that the load voltage is a nearly perfect sinusoid with total harmonic distortion of 0.85 %.

2.8 Experimental Results of the Proposed System with Linear Loads

A prototype experimental module of the proposed UPS system was constructed in the laboratory to verify the operation of the control strategy. Toshiba giant insulated gate bipolar transistors (IGBT) modules (MG50H2YS1) were employed as the power switching devices.

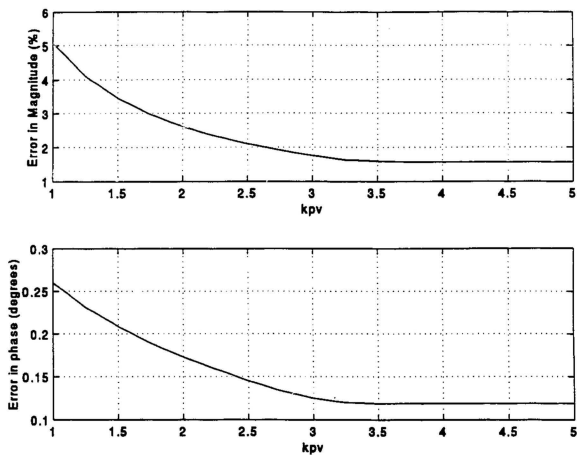


Figure 2.23: Error in the magnitude and phase of the capacitor voltage with respect to its reference waveform

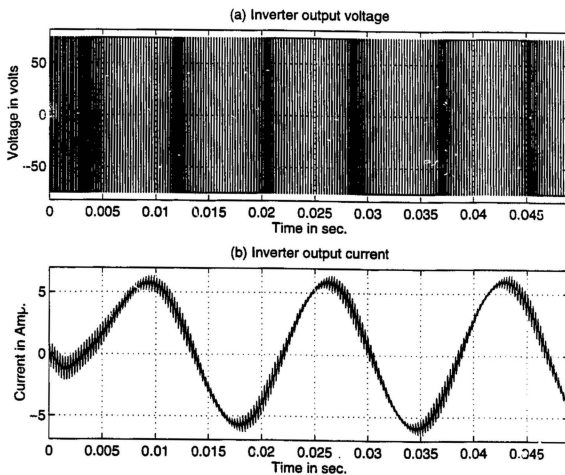


Figure 2.24: Time-domain simulation of the inverter output voltage and current of the proposed control scheme with $k_{pc}=2.0$ and $k_{pv}=2.75$

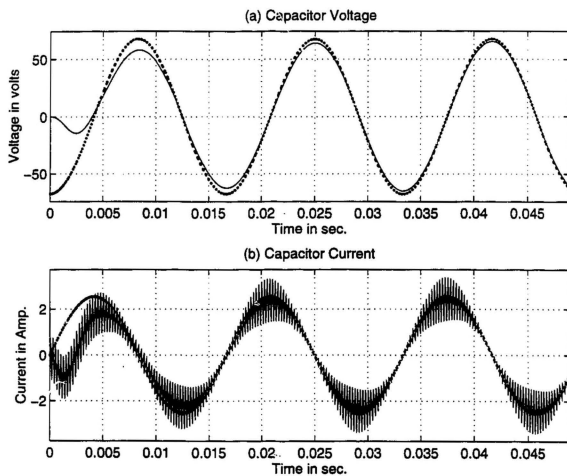


Figure 2.25: Time-domain simulation of the capacitor voltage and current of the proposed control scheme with $k_{pc}=2.0$ and $k_{pv}=2.75$

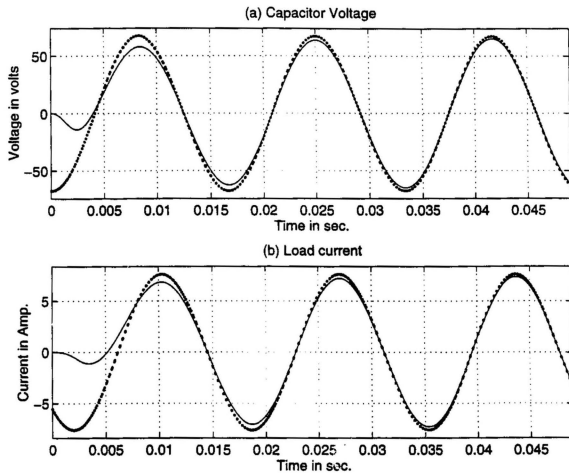


Figure 2.26: Time-domain simulation of the load current of the proposed control scheme with $k_{pc}=2.0$ and $k_{pv}=2.75$

Figure 2.27 shows the experimental waveforms of the inverter output voltage and current. The inverter output current (lower trace) was recorded by observing the voltage drop across a non-inductive current shunt of 10 m Ω resistance. The upper trace shows that the inverter output voltage is a pulse-width modulated waveform with variable width and superimposed high-frequency harmonics. Figure 2.27 shows close agreement with the simulated waveforms of Fig. 2.24.

Figure 2.28 shows the steady-state waveforms of the load (capacitor) voltage and load current. The figure shows that both the load voltage and current are nearly perfect sinusoids. The measured THD of the load voltage is 2.1 %. Figure 2.29 shows the inverter output voltage and load voltage. The figure shows that the voltage gain is 80 % of the input DC voltage. This value is lower than the predicted value of 87 %. The discrepancy arises from the adverse effect of dead- or blanking-time intervals in the inverter output voltage. Higher voltage gains can be achieved by compensating for the effect of dead-time intervals [108]-[110]. Figure 2.30 shows the steady-state capacitor voltage and current waveforms. The figure shows that the capacitor acts as a trap for higher-order harmonics.

The transient response of the capacitor voltage and current from “cold” start to full load is depicted in Fig. 2.31. The upper trace shows the capacitor voltage and the lower trace shows the capacitor current. The figure shows that the capacitor voltage takes about half cycle to reach steady state, indicating fast transient response. Figure 2.32 shows the system dynamic response for 100 % step change in the load from no-load to full-load and vice-versa. The figure shows that the system exhibits very fast dynamic response with excellent load-voltage regulation and very little change in the load voltage at the point of applying or removing the full load. Thus, the control

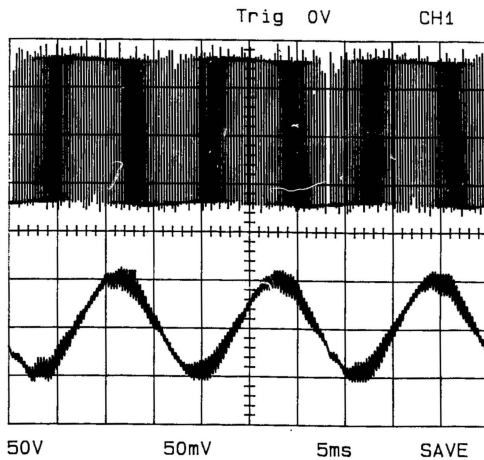


Figure 2.27: Experimental waveforms of the steady-state inverter output voltage (upper trace) and current (lower trace)

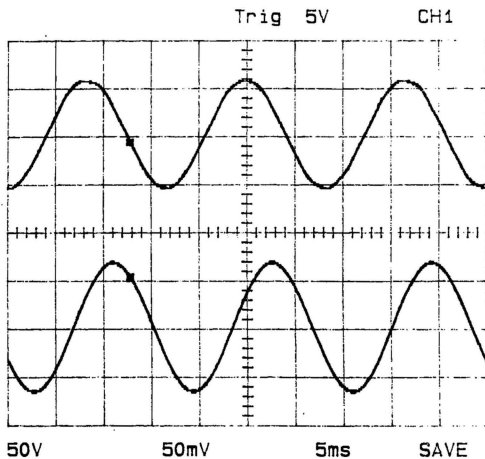


Figure 2.28: Experimental waveforms of the steady-state capacitor voltage (upper trace) and load current (lower trace)

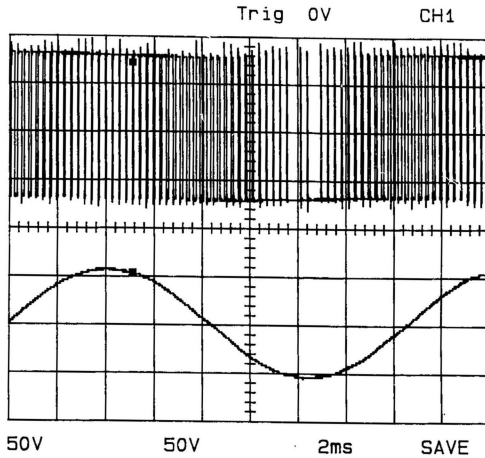


Figure 2.29: Experimental waveforms of the steady-state inverter output voltage and load voltage, upper trace: inverter output voltage, lower trace: load voltage

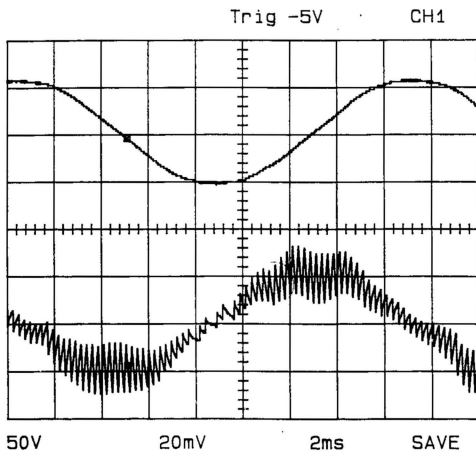


Figure 2.30: Experimental waveforms of the steady-state capacitor voltage and current, upper trace: capacitor voltage, lower trace: capacitor current

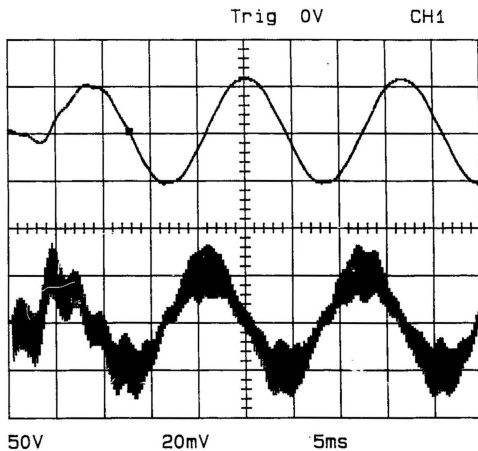
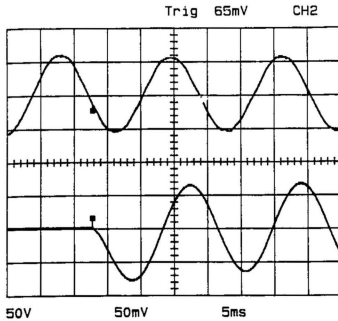
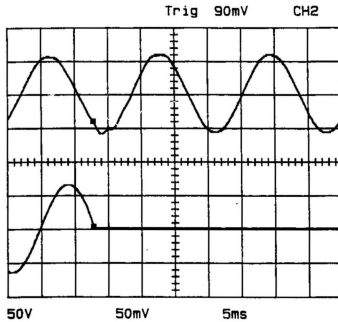


Figure 2.31: Experimental waveforms of the transient response load of the voltage from "cold" start to full-load, upper trace: load voltage, lower trace: capacitor current



(a)



(b)

Figure 2.32: Experimental waveforms of the dynamic response of the capacitor voltage for 100% step change in the load: a) 100 % application of the load, upper trace: load voltage, lower trace: load current, b) 100 % removal of the load, upper trace: load voltage, lower trace: load current

scheme ensures a “stiff” load voltage.

2.9 Experimental Results of the Proposed System with Non-Linear Loads

The performance of the proposed UPS was examined for non-linear loads. The non-linear load was chosen as a full-bridge rectifier with R-C load at the DC side of the bridge rectifier as shown in Fig. 2.33. The load parameters were chosen as $R_{dc} =$

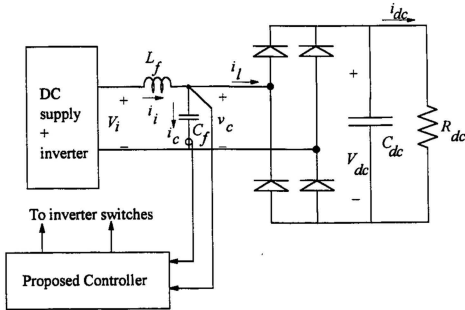


Figure 2.33: Schematic diagram of the proposed scheme with non-linear load

$10 \, \Omega$, $C_{dc} = 2500 \, \mu\text{F}$.

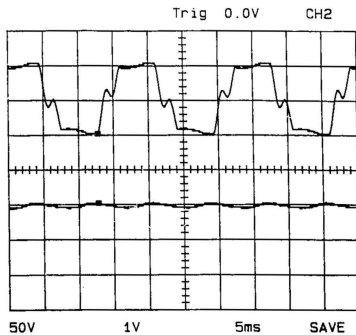
Figures 2.34 to Fig. 2.36 show the waveforms of the output voltage of the UPS system, the output voltage of the bridge rectifier, the current drawn by the non-linear load from the UPS system, and the current drawn by the load at the output of the bridge rectifier for three values of the filter capacitor. The figures show that the input voltage to the bridge rectifier is somewhat distorted. However, the voltage waveshape improves with increasing values of C_f .

2.10 Summary

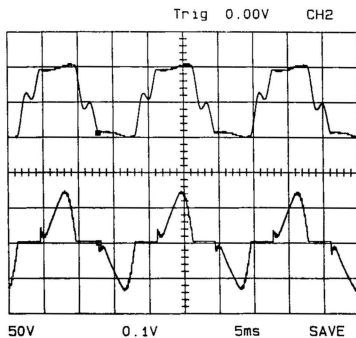
A current-regulated voltage-controlled scheme for single-phase voltage-source UPS system was developed in this chapter. A general model of the single-phase UPS system was first established using state-space representation.

Using Fourier series approach, the discontinuous forcing function in the system state-space representation was replaced by its Fourier series components. Two time-continuous models (the low-frequency and high-frequency models) were derived and used to select optimum filter parameters for the power circuit. Based on the normalized rating of the filter inductor and capacitor, the attenuation in the fundamental component in the inverter output voltage, and the total harmonic distortion of the load voltage, optimum filter parameters of $X_{lfm} = 0.18$ pu, and $X_{cfm} = 2.5$ pu were selected.

In order to examine the dynamic behaviour of the system, a linear small-signal dynamic model was derived from the low-frequency model using perturbation and small-signal approximation. The small-signal dynamic model was then used to assess the incremental dynamics of the power circuit and examine the stability of the feedback system using the root-locus technique. It was shown that choosing the load

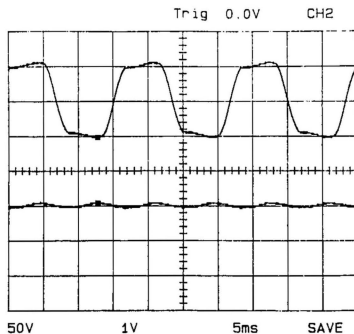


(a)

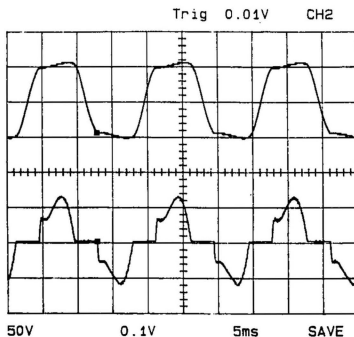


(b)

Figure 2.34: Experimental waveforms of the proposed scheme for non-linear loads with $C_f=100.0 \mu\text{F}$: a) upper trace: v_c , lower trace: i_{dc} , b) upper trace: v_c , lower trace: i_l

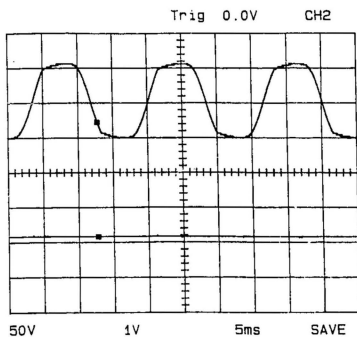


(a)

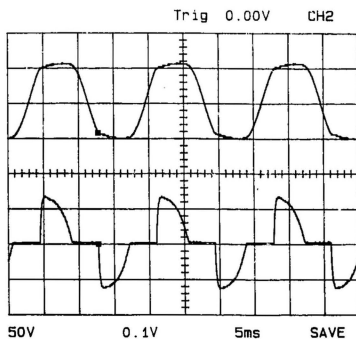


(b)

Figure 2.35: Experimental waveforms of the proposed scheme for non-linear loads with $C_f=600.0 \mu\text{F}$: a) upper trace: v_c , lower trace: i_{dc} , b) upper trace: v_c , lower trace: i_l



(a)



(b)

Figure 2.36: Experimental waveforms of the proposed scheme with $C_f=900.0 \mu\text{F}$: a) upper trace: v_c , lower trace: i_{dc} , b) upper trace: v_c , lower trace: i_l

(capacitor) voltage as the feedback variable in the control circuit results in an oscillatory behaviour of the UPS system. However, choosing either the capacitor or inverter output current as the feedback variable in the UPS system produces stable operation. Selection of the inverter output current as the feedback variable was overruled because of possible harmonic instability in the load circuit or the need for an extra load current sensor. Hence, the capacitor current was chosen as the feedback variable for stable operation of the single-phase UPS. An outer voltage feedback loop was incorporated to ensure successful operation of the UPS system and obtain sinusoidal load voltage which faithfully tracks its reference signal. It was shown that proportional controllers in the feed-forward path of both the inner and outer feedback loops were sufficient to produce well-regulated, nearly-perfect sinusoidal load voltage, and excellent dynamic performance of the UPS system.

Experimental results from a laboratory prototype module for both linear and non-linear loads were presented. The results for the linear loads agreed well with the simulation results and the theoretical results obtained from the derived models, thus validating the analytical procedures. The results with non-linear loads show that the proposed scheme is compatible with non-linear loads. However, higher values of the filter capacitor are required to provide low THD.

Chapter 3

The Three-Phase Voltage-Source Uninterruptible Power Supply System

This chapter deals with the modeling and analysis of the three-phase voltage-source UPS system with the proposed control strategy presented for the single-phase UPS system. At the onset, a general model of the three-phase UPS power circuit with the input DC filter dynamics taken into account is developed. Employing the Fourier series technique, an averaged low-frequency time-continuous model is derived from the general model. In order to cope with the time-varying nature of the system matrix, the system variables are transformed to a rotating frame of reference using the forward-backward transformation. The result is a time-invariant, but non-linear model of the three-phase UPS power circuit.

Perturbation and small-signal analysis technique are used to develop steady-state and dynamic models of the power circuit in the rotating frame of reference. The steady-state equations represent the nominal operating condition around which the small-signal model is derived. The small-signal model is employed to obtain transfer functions relating the incremental variation of the power circuit state variables to

incremental changes in the control signal. It is shown, through pole-zero maps and root-locus analysis, that the control scheme proposed for the single-phase UPS system results in stable operation of the three-phase UPS system. Computer simulation of the three-phase UPS system along with experimental verification of the proposed three-phase UPS system are presented in the chapter.

3.1 General Model of the Three-phase UPS Circuit

Figure 3.1 shows the power circuit of the three-phase voltage-source UPS. It consists of a second-order DC input filter (L_s - C_d), a three-phase full-bridge voltage-source inverter, a second-order AC filter (L_f - C_f), and a balanced three-phase r_l - l_l load. The input filter is employed to ensure a smooth DC voltage at the input of the power inverter. From Fig. 3.1, the current drawn from the input DC source is given by

$$i_s = i_{cd} + i_d. \quad (3.1)$$

i_d is obtained in terms of the switching functions as

$$i_d = S_a^* i_{ia} + S_b^* i_{ib} + S_c^* i_{ic}, \quad (3.2)$$

where, for example in inverter leg of *phase a*, $S_a^* = 1$ when S_a is ON (i.e., S'_a is OFF) and $S_a^* = 0$ when S_a is OFF (i.e., S'_a is ON). Similar conditions apply for inverter legs of *phases b* and *c*.

The current i_{cd} is given by

$$i_{cd} = C_d \frac{dv_d}{dt}. \quad (3.3)$$

Substituting Eqs. (3.2) and (3.3) into (3.1), yields

$$C_d \frac{dv_d}{dt} = i_s - (S_a^* i_{ia} + S_b^* i_{ib} + S_c^* i_{ic}). \quad (3.4)$$

$$C_f \frac{dv_{can}}{dt} = i_{ca} = i_{ia} - i_{la}. \quad (3.8)$$

Similarly, the governing differential equations for *phase b* can be written as

$$L_f \frac{di_{ib}}{dt} + i_{ib} R_f = S_b^* v_d - v_{cbn} - v_{ng}, \quad (3.9)$$

$$l_l \frac{di_{lb}}{dt} + i_{lb} r_l = v_{cbn}, \quad (3.10)$$

$$C_f \frac{dv_{cbn}}{dt} = i_{cb} = i_{ib} - i_{lb}. \quad (3.11)$$

And, for *phase c*

$$L_f \frac{di_{ic}}{dt} + i_{ic} R_f = S_c^* v_d - v_{ccn} - v_{ng}, \quad (3.12)$$

$$l_l \frac{di_{lc}}{dt} + i_{lc} r_l = v_{ccn}, \quad (3.13)$$

$$C_f \frac{dv_{ccn}}{dt} = i_{cc} = i_{ic} - i_{lc}. \quad (3.14)$$

Summing Eqs. (3.6), (3.9), and (3.12), the voltage v_{ng} is obtained in terms of the states of the power switches as

$$v_{ng} = \frac{v_d}{3} (S_a^* + S_b^* + S_c^*). \quad (3.15)$$

Equation (3.15) was obtained assuming a balanced three-phase load; i.e.,

$$v_{can} + v_{cbn} + v_{ccn} = 0, \quad (3.16)$$

$$i_{ia} + i_{ib} + i_{ic} = 0. \quad (3.17)$$

Substituting Eq. (3.15) into Eqs. (3.6), (3.9), and (3.12), results in the following equations:

$$L_f \frac{di_{ia}}{dt} + R_f i_{ia} = v_d (S_a^* - \frac{1}{3} (S_a^* + S_b^* + S_c^*)) - v_{can}, \quad (3.18)$$

$$L_f \frac{di_{ib}}{dt} + R_f i_{ib} = v_d (S_b^* - \frac{1}{3} (S_a^* + S_b^* + S_c^*)) - v_{cbn}, \quad (3.19)$$

$$L_f \frac{di_{ic}}{dt} + R_f i_{ic} = v_d (S_c^* - \frac{1}{3} (S_a^* + S_b^* + S_c^*)) - v_{ccn}. \quad (3.20)$$

The system equations can be written in a state-space representation as

$$\dot{\mathbf{x}} = \mathbf{A}^* \mathbf{x} + \mathbf{B} \mathbf{e}; \quad (3.21)$$

i.e.,

$$\begin{bmatrix} \dot{i}_{ia} \\ \dot{i}_{ia} \\ \dot{v}_{can} \\ \dot{i}_{ib} \\ \dot{i}_{ib} \\ \dot{v}_{cbn} \\ \dot{i}_{ic} \\ \dot{i}_{ic} \\ \dot{v}_{ccn} \\ \dot{i}_s \\ \dot{v}_d \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{r_l}{l_l} & \frac{1}{l_l} & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{l_l} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{r_l}{l_l} & \frac{1}{l_l} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_f} & -\frac{1}{C_f} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{S_a^*}{C_d} & 0 & 0 & -\frac{S_a^*}{C_d} & 0 & 0 & -\frac{S_b^*}{C_d} & 0 & 0 \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ -\frac{R_s}{L_s} \\ -\frac{1}{C_d} \end{bmatrix} + \begin{bmatrix} \frac{S_a^* - \frac{1}{3}(S_a^* + S_b^* + S_c^*)}{L_f} \\ 0 \\ 0 \\ \frac{S_b^* - \frac{1}{3}(S_a^* + S_b^* + S_c^*)}{L_f} \\ 0 \\ 0 \\ 0 \\ \frac{S_c^* - \frac{1}{3}(S_a^* + S_b^* + S_c^*)}{L_f} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} i_{ia} \\ i_{ia} \\ v_{can} \\ i_{ib} \\ i_{ib} \\ v_{cbn} \\ i_{ic} \\ i_{ic} \\ v_{ccn} \\ i_s \\ v_d \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \frac{1}{L_s} \\ 0 \end{bmatrix} v_{dc}. \quad (3.22)$$

For simplicity, the product term $\mathbf{B} \mathbf{e}$ is evaluated and denoted by the vector \mathbf{u} .

Equation (3.22) can be solved to obtain the exact solution for the system state variables at any instant in time provided the switching functions S_a^* , S_b^* , S_c^* are defined. It, therefore, represents the general state-space model of the three-phase UPS and can be solved numerically to obtain various waveforms in the power circuit. In

this thesis, however, an analytical approach is preferred since it leads to models which can be used to investigate the performance of the three-phase UPS system using well-established techniques. The details of developing these models are presented in the next section.

3.2 Low-Frequency Model in the Stationary Frame of Reference

For an inverter switching frequency much higher than that of the modulating signal, the discrete switching functions S_a^* , S_b^* , and S_c^* can be approximated by their corresponding time-average functions (i.e. duty cycle), d_a , d_b , and d_c , which are described as (Eq. (2.18))

$$d_a = \frac{m \cos(\omega t) + 1}{2}, \quad (3.23)$$

$$d_b = \frac{m \cos(\omega t - \frac{2\pi}{3}) + 1}{2}, \quad (3.24)$$

$$d_c = \frac{m \cos(\omega t + \frac{2\pi}{3}) + 1}{2}. \quad (3.25)$$

Replacing the discrete switching functions by their corresponding average values, Eq. (3.22) can be written as

$$\dot{\mathbf{x}} = \mathbf{A} \mathbf{x} + \mathbf{u}, \quad (3.26)$$

or,

$$\begin{bmatrix} \dot{i}_{ia} \\ \dot{i}_{la} \\ \dot{v}_{can} \\ \dot{i}_{ib} \\ \dot{i}_{lb} \\ \dot{v}_{cbn} \\ \dot{i}_{ic} \\ \dot{i}_{lc} \\ \dot{v}_{ccn} \\ \dot{i}_s \\ \dot{v}_d \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & 0 & 0 & 0 \\ 0 & -\frac{r_l}{l_l} & \frac{1}{l_l} & 0 & 0 & 0 & 0 \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 \\ 0 & 0 & 0 & 0 & -\frac{r_l}{l_l} & \frac{1}{l_l} & 0 \\ 0 & 0 & 0 & \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{R_f}{L_f} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_f} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{m \cos \omega t + 1}{2C_d} & 0 & 0 & -\frac{m \cos(\omega t - \frac{2\pi}{3}) + 1}{2C_d} & 0 & 0 & -\frac{m \cos(\omega t + \frac{2\pi}{3}) + 1}{2C_d} \end{bmatrix} \begin{bmatrix} i_{ia} \\ i_{la} \\ v_{can} \\ i_{ib} \\ i_{lb} \\ v_{cbn} \\ i_{ic} \\ i_{lc} \\ v_{ccn} \\ i_s \\ v_d \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \frac{v_{dc}}{L_s} \\ 0 \end{bmatrix} \quad (3.27)$$

Equation (3.27) describes the general state-space averaged model of the three-phase UPS system. The following can be deduced from the equation:

1. if the inverter input filter is neglected, Eq. (3.27) reduces to [111]

$$\begin{bmatrix} \dot{i}_{ia} \\ \dot{i}_{la} \\ \dot{v}_{can} \\ \dot{i}_{ib} \\ \dot{i}_{lb} \\ \dot{v}_{cbn} \\ \dot{i}_{ic} \\ \dot{i}_{lc} \\ \dot{v}_{ccn} \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{r_l}{l_l} & \frac{1}{l_l} & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_f} & -\frac{r_l}{C_f} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{r_l}{l_l} & \frac{1}{l_l} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_f} & -\frac{r_l}{C_f} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{r_l}{l_l} & \frac{1}{l_l} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_f} & -\frac{r_l}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_{ia} \\ i_{la} \\ v_{can} \\ i_{ib} \\ i_{lb} \\ v_{cbn} \\ i_{ic} \\ i_{lc} \\ v_{ccn} \end{bmatrix} + \begin{bmatrix} \frac{m v_{dc} \cos \omega t}{2 L_f} \\ 0 \\ 0 \\ \frac{m v_{dc} \cos(\omega t - \frac{2\pi}{3})}{2 L_f} \\ 0 \\ 0 \\ \frac{m v_{dc} \cos(\omega t - \frac{2\pi}{3})}{2 L_f} \\ 0 \\ 0 \end{bmatrix}. \quad (3.28)$$

Equation (3.28) shows that the system has controlled sinusoidal forcing functions whose amplitudes are given by the product of the modulation index m and the input DC voltage v_{dc} . For a maximum modulation index of unity, the inverter output has a maximum line-to-line voltage of $\frac{\sqrt{3}}{2} v_{dc}$.

2. the **A** matrix in Eq. (3.28) is time-invariant.
3. Equation (3.27) shows that phase interactions exist if the input filter is taken into account. Equation (3.28), on the other hand, shows that the state variables of the three phases are completely decoupled if the input filter is neglected and balanced three-phase load is assumed. For this case, the three-phase system can

be analyzed on a per-phase basis, similar to the analysis presented in Chapter Two.

3.3 Low-Frequency Model in the Rotating Frame of Reference

Upon examining Eq. (3.27), it can be seen that the system matrix is time-varying. The time-varying nature of the system model makes it difficult to obtain a closed-form solution for the system state variables. However, this difficulty can be overcome by transforming the system variables to a rotating frame of reference which is synchronized and in-phase with the modulating signals.

The transformation to the rotating frame of reference is achieved by using the forward-backward transformation [112]. The state vector in the rotating frame of reference, \mathbf{x}_r , is related to its counterpart in the stationary frame of reference by the transformation matrix \mathbf{T} such that

$$\mathbf{x}_r = \mathbf{T} \mathbf{x}. \quad (3.29)$$

Similarly, the input vector in the rotating and stationary frame of reference is related by

$$\mathbf{u}_r = \mathbf{T} \mathbf{u}. \quad (3.30)$$

The state and input vectors in the stationary frame of reference can be obtained from Eq. (3.29) and (3.30) by post-multiplying the corresponding equation by the inverse of the transformation matrix \mathbf{T}^{-1} ; i.e.,

$$\mathbf{x} = \mathbf{T}^{-1} \mathbf{x}_r, \quad (3.31)$$

$$\mathbf{u} = \mathbf{T}^{-1} \mathbf{u}_r. \quad (3.32)$$

The forward-backward transformation matrix \mathbf{T} and its inverse \mathbf{T}^{-1} are given by:

$$\mathbf{T} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 \\ e^{j\omega t} & 0 & 0 & e^{j(\omega t - \frac{2\pi}{3})} & 0 & 0 \\ 0 & e^{j\omega t} & 0 & 0 & e^{j(\omega t - \frac{2\pi}{3})} & 0 \\ 0 & 0 & e^{j\omega t} & 0 & 0 & e^{j(\omega t - \frac{2\pi}{3})} \\ e^{-j\omega t} & 0 & 0 & e^{-j(\omega t - \frac{2\pi}{3})} & 0 & 0 \\ 0 & e^{-j\omega t} & 0 & 0 & e^{-j(\omega t - \frac{2\pi}{3})} & 0 \\ 0 & 0 & e^{-j\omega t} & 0 & 0 & e^{-j(\omega t - \frac{2\pi}{3})} \\ 1 & 0 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 & 0 \end{bmatrix}, \quad (3.33)$$

$$\mathbf{T}^{-1} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 0 & 0 & e^{-j\omega t} & 0 & 0 & e^{j\omega t} \\ 0 & 1 & 0 & 0 & e^{-j\omega t} & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & e^{-j\omega t} & 0 \\ 1 & 0 & 0 & e^{-j(\omega t - 120)} & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & e^{-j(\omega t - 120)} & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & e^{-j(\omega t - 120)} & e^{j(\omega t + 120)} \\ 1 & 0 & 0 & e^{-j(\omega t + 120)} & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & e^{-j(\omega t + 120)} & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & e^{-j(\omega t + 120)} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$\begin{bmatrix}
 0 & 0 & 0 & 0 \\
 e^{j\omega t} & 0 & 0 & 0 \\
 0 & e^{j\omega t} & 0 & 0 \\
 e^{j(\omega t-120)} & 0 & 0 & 0 \\
 0 & e^{j(\omega t-120)} & 0 & 0 \\
 0 & 0 & 0 & 0 \\
 e^{j(\omega t+120)} & 0 & 0 & 0 \\
 0 & e^{j(\omega t+120)} & 0 & 0 \\
 0 & 0 & \sqrt{3} & 0 \\
 0 & 0 & 0 & \sqrt{3}
 \end{bmatrix} \quad (3.34)$$

The system state variables in the rotating frame of reference are obtained by substituting Eq. (3.33) into (3.29), giving

$$\begin{bmatrix}
 i_{i0} \\
 i_{i0} \\
 v_{c0} \\
 i_{iF} \\
 i_{iF} \\
 v_{cF} \\
 i_{iB} \\
 i_{iB} \\
 v_{cB} \\
 i_s \\
 v_d
 \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix}
 i_{ia} + i_{ib} + i_{ic} \\
 i_{ia} + i_{ib} + i_{ic} \\
 v_{can} + v_{cbn} + v_{ccn} \\
 i_{ia} e^{j\omega t} + i_{ib} e^{j(\omega t - \frac{2\pi}{3})} + i_{ic} e^{j(\omega t + \frac{2\pi}{3})} \\
 i_{ia} e^{j\omega t} + i_{ib} e^{j(\omega t - \frac{2\pi}{3})} + i_{ic} e^{j(\omega t + \frac{2\pi}{3})} \\
 v_{can} e^{j\omega t} + v_{cbn} e^{j(\omega t - \frac{2\pi}{3})} + v_{ccn} e^{j(\omega t + \frac{2\pi}{3})} \\
 i_{ia} e^{-j\omega t} + i_{ib} e^{-j(\omega t - \frac{2\pi}{3})} + i_{ic} e^{-j(\omega t + \frac{2\pi}{3})} \\
 i_{ia} e^{-j\omega t} + i_{ib} e^{-j(\omega t - \frac{2\pi}{3})} + i_{ic} e^{-j(\omega t + \frac{2\pi}{3})} \\
 v_{can} e^{-j\omega t} + v_{cbn} e^{-j(\omega t - \frac{2\pi}{3})} + v_{ccn} e^{-j(\omega t + \frac{2\pi}{3})} \\
 \sqrt{3} i_s \\
 \sqrt{3} v_d
 \end{bmatrix}, \quad (3.35)$$

where the subscripts F and B represent the forward and backward components respectively.

It can be seen from the 10th and 11th rows of Eq. (3.35) that the DC state variables i_s and v_d are not affected by the transformation.

Similarly, the input vector in the rotating frame of reference is given by

$$\mathbf{u}_r = \left[0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ \frac{V_d}{L_s} \ 0 \right]^T. \quad (3.36)$$

The system state-space equations in the rotating frame of reference are obtained

by substituting Eqs. (3.31) and (3.32) into (3.26) to give

$$\frac{d}{dt}(\mathbf{T}^{-1} \mathbf{x}_r) = \mathbf{A} \mathbf{T}^{-1} \mathbf{x}_r + \mathbf{T}^{-1} \mathbf{u}_r, \quad (3.37)$$

$$(\dot{\mathbf{T}})^{-1} \mathbf{x}_r + \mathbf{T}^{-1} \dot{\mathbf{x}}_r = \mathbf{A} \mathbf{T}^{-1} \mathbf{x}_r + \mathbf{T}^{-1} \mathbf{u}_r, \quad (3.38)$$

$$\mathbf{T}^{-1} \dot{\mathbf{x}}_r = (\mathbf{A} \mathbf{T}^{-1} - (\dot{\mathbf{T}})^{-1}) \mathbf{x}_r + \mathbf{T}^{-1} \mathbf{u}_r. \quad (3.39)$$

Post multiplying Eq. (3.39) by \mathbf{T} , the system state-space equations in the rotating frame of reference can be written as

$$\dot{\mathbf{x}}_r = \mathbf{A}_r \mathbf{x}_r + \mathbf{u}_r, \quad (3.40)$$

where

$$\mathbf{A}_r = \mathbf{T} \mathbf{A} \mathbf{T}^{-1} - \mathbf{T} (\dot{\mathbf{T}})^{-1}. \quad (3.41)$$

The system matrix in Eq. (3.40), \mathbf{A}_r , is obtained by substituting the \mathbf{A} matrix from Eq. (3.27) and the transformation matrices \mathbf{T} and \mathbf{T}^{-1} from Eqs. (3.33) and (3.34) respectively into Eq. (3.41).

The system state-space equation in the rotating frame of reference is obtained from Eq. (3.40) as

$$\begin{bmatrix} \dot{i}_{i0} \\ \dot{i}_{j0} \\ \dot{v}_{c0} \\ \dot{i}_{iF} \\ \dot{i}_{jF} \\ \dot{v}_{cF} \\ \dot{i}_{iB} \\ \dot{i}_{jB} \\ \dot{v}_{cB} \\ \dot{i}_s \\ \dot{v}_d \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & 0 & 0 \\ 0 & -\frac{r_L}{l_i} & \frac{1}{l_i} & 0 & 0 & 0 \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_f}{L_f} + j\omega & 0 & -\frac{1}{L_f} \\ 0 & 0 & 0 & 0 & -\frac{r_L}{l_i} + j\omega & \frac{1}{l_i} \\ 0 & 0 & 0 & \frac{1}{C_f} & -\frac{1}{C_f} & j\omega \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{\sqrt{3}m}{4C_d} & 0 & 0 & -\frac{\sqrt{3}m}{4C_d} & 0 & 0 \end{bmatrix}$$

$$\begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{\sqrt{3}m}{4L_f} \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
-\frac{R_f}{L_f} - j\omega & 0 & -\frac{1}{L_f} & 0 & \frac{\sqrt{3}m}{4L_f} \\
0 & -\frac{r_l}{l_l} - j\omega & \frac{1}{l_l} & 0 & 0 \\
\frac{1}{C_f} & -\frac{1}{C_f} & -j\omega & 0 & 0 \\
0 & 0 & 0 & -\frac{R_s}{L_s} & -\frac{1}{L_s} \\
-\frac{\sqrt{3}m}{4C_d} & 0 & 0 & \frac{1}{C_d} & 0
\end{bmatrix}
\begin{bmatrix}
i_{i0} \\
i_{l0} \\
v_{c0} \\
i_{iF} \\
i_{lF} \\
v_{cF} \\
i_{iB} \\
i_{lB} \\
v_{cB} \\
i_s \\
v_d
\end{bmatrix}
+
\begin{bmatrix}
0 \\
0 \\
0 \\
0 \\
0 \\
0 \\
0 \\
0 \\
0 \\
\frac{v_{dc}}{L_s} \\
0
\end{bmatrix}.
\quad (3.42)$$

Equation (3.42) was computed using the symbolic computation package MAPLE [106, 107]. The Equation shows that the system model in the rotating frame of reference is time-invariant.

For a balanced three-phase load, the zero-sequence component of the state variables are zero, and the system equations can be represented by the equation

$$\dot{\mathbf{x}}_{rr} = \mathbf{A}_{rr} \mathbf{x}_{rr} + \mathbf{u}_{rr}, \quad (3.43)$$

where the subscript rr denotes the reduced order in the rotating frame of reference.

Equation (3.43) can be rewritten as

$$\begin{bmatrix}
\dot{i}_{iF} \\
\dot{i}_{lF} \\
\dot{v}_{cF} \\
\dot{i}_{iB} \\
\dot{i}_{lB} \\
\dot{v}_{cB} \\
\dot{i}_s \\
\dot{v}_d
\end{bmatrix}
=
\begin{bmatrix}
-\frac{R_f}{L_f} + j\omega & 0 & -\frac{1}{L_f} & 0 & 0 & 0 \\
0 & -\frac{r_l}{l_l} + j\omega & \frac{1}{l_l} & 0 & 0 & 0 \\
\frac{1}{C_f} & -\frac{1}{C_f} & j\omega & 0 & 0 & 0 \\
0 & 0 & 0 & -\frac{R_f}{L_f} - j\omega & 0 & -\frac{1}{L_f} \\
0 & 0 & 0 & 0 & -\frac{r_l}{l_l} - j\omega & -\frac{1}{l_l} \\
0 & 0 & 0 & \frac{1}{C_f} & -\frac{1}{C_f} & -j\omega \\
0 & 0 & 0 & 0 & 0 & 0 \\
-\frac{\sqrt{3}m}{4C_d} & 0 & 0 & -\frac{\sqrt{3}m}{4C_d} & 0 & 0
\end{bmatrix}$$

$$\begin{bmatrix} 0 & \frac{\sqrt{3}m}{4L_f} \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{\sqrt{3}m}{4L_f} \\ 0 & 0 \\ 0 & 0 \\ -\frac{R_s}{L_s} & -\frac{1}{L_s} \\ \frac{1}{C_d} & 0 \end{bmatrix} \begin{bmatrix} i_{iF} \\ i_{lF} \\ v_{cF} \\ i_{iB} \\ i_{lB} \\ v_{cB} \\ i_s \\ v_d \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \frac{v_{dc}}{L_s} \\ 0 \end{bmatrix}. \quad (3.44)$$

Upon examining Eqs. (3.22) and (3.44), it can be seen that through the averaging of the switching functions and the transformation of the state variables to the rotating frame of reference, the discontinuous model of the system (Eq. (3.22)) has been approximated by a state-space averaged model that is continuous and time-invariant (Eq. (3.44)). However, the resulting system state-space averaged model is non-linear. This is evident from the presence of the terms $\frac{\sqrt{3}m i_{iF}}{4C_d}$, $\frac{\sqrt{3}m i_{iB}}{4C_d}$, and $\frac{\sqrt{3}m v_d}{4C_d}$ in Eq. (3.44). Thus, to solve for the system steady-state variables and obtain an analytical model which describes the system dynamic behaviour, the system model has to be linearized.

3.4 Linearized Model in the Rotating Frame of Reference

The system model given by Eq. (3.44) is linearized by using the perturbation technique and small-signal approximation. The state variables are perturbed around their nominal operating point, and are represented by

$$\mathbf{x}_{rr} = \mathbf{X}_{rr} + \tilde{\mathbf{x}}_{rr}; \quad (3.45)$$

i.e.,

$$\begin{bmatrix} i_{iF} \\ i_{lF} \\ v_{cF} \\ i_{iB} \\ i_{lB} \\ v_{cB} \\ i_{is} \\ v_d \end{bmatrix} = \begin{bmatrix} I_{iF} \\ I_{lF} \\ V_{cF} \\ I_{iB} \\ I_{lB} \\ V_{iB} \\ I_{is} \\ V_d \end{bmatrix} + \begin{bmatrix} \tilde{i}_{iF} \\ \tilde{i}_{lF} \\ \tilde{v}_{cF} \\ \tilde{i}_{iB} \\ \tilde{i}_{lB} \\ \tilde{v}_{iB} \\ \tilde{i}_{is} \\ \tilde{v}_d \end{bmatrix}, \quad (3.46)$$

where the upper case letters denote nominal values and $\tilde{i}_{iF}, \tilde{i}_{lF}, \dots$ denote small excursions from the nominal operating point.

Similarly, the perturbed model for the modulating signal, the input DC source, and the load circuit, $r_l - l_l$ are given respectively by:

$$m = M + \tilde{m}, \quad (3.47)$$

$$v_{dc} = V_{dc} + \tilde{v}_{dc}, \quad (3.48)$$

$$r_l = R_l + \tilde{r}_l, \quad (3.49)$$

$$l_l = L_l + \tilde{l}_l. \quad (3.50)$$

Substituting Eqs. (3.46) to (3.50) into Eq. (3.44) gives

$$\frac{d}{dt} \begin{bmatrix} I_{if} + \tilde{i}_{if} \\ I_{lf} + \tilde{i}_{lf} \\ V_{cf} + \tilde{v}_{cf} \\ I_{ib} + \tilde{i}_{ib} \\ I_{lb} + \tilde{i}_{lb} \\ V_{cb} + \tilde{v}_{cb} \\ I_s + \tilde{i}_s \\ V_d + \tilde{v}_d \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} + j\omega & 0 & \frac{1}{L_f} & 0 & 0 \\ 0 & -\frac{R_l + \tilde{r}_l}{L_l + \tilde{l}_l} + j\omega & \frac{1}{L_l + \tilde{l}_l} & 0 & 0 \\ \frac{1}{C_f} & -\frac{1}{C_f} & j\omega & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_f}{L_f} - j\omega & 0 \\ 0 & 0 & 0 & 0 & -\frac{R_l + \tilde{r}_l}{L_l + \tilde{l}_l} - j\omega \\ 0 & 0 & 0 & \frac{1}{C_f} & -\frac{1}{C_f} \\ 0 & 0 & 0 & 0 & 0 \\ -\frac{\sqrt{3}(M + \tilde{m})}{4C_d} & 0 & 0 & -\frac{\sqrt{3}(M + \tilde{m})}{4C_d} & 0 \end{bmatrix}$$

$$\begin{bmatrix}
0 & 0 & \frac{\sqrt{3}(M+\tilde{m})}{4L_f} \\
0 & 0 & 0 \\
0 & 0 & 0 \\
0 & 0 & \frac{\sqrt{3}(M+\tilde{m})}{4L_f} \\
\frac{1}{L_l + \tilde{l}_l} & 0 & 0 \\
-j\omega & 0 & 0 \\
0 & -\frac{R_s}{L_s} & -\frac{1}{L_s} \\
0 & \frac{1}{C_d} & 0
\end{bmatrix}
\begin{bmatrix}
I_{if} + \tilde{i}_{if} \\
I_{lf} + \tilde{i}_{lf} \\
V_{cf} + \tilde{v}_{cf} \\
I_{ib} + \tilde{i}_{ib} \\
I_{lb} + \tilde{i}_{lb} \\
V_{cb} + \tilde{v}_{cb} \\
I_s + \tilde{i}_s \\
V_d + \tilde{v}_d
\end{bmatrix}
+
\begin{bmatrix}
0 \\
0 \\
0 \\
0 \\
0 \\
0 \\
\frac{V_{dc} + \tilde{v}_{dc}}{L_s} \\
0
\end{bmatrix} \quad (3.51)$$

An approximate representation of Eq. (3.51) can be obtained by assuming that the perturbation is sufficiently small so that higher-order and cross-product (non-linear) terms of the small-signal variables can be neglected. For example, the element (2,2) of the system matrix in Eq. (3.51) can be approximated as,

$$-\frac{R_l + \tilde{r}_l}{L_l + \tilde{l}_l} + j\omega = -\frac{R_l}{L_l} \left(1 + \frac{\tilde{r}_l}{R_l}\right) \left(1 + \frac{\tilde{l}_l}{L_l}\right)^{-1} + j\omega, \quad (3.52)$$

$$\cong -\frac{R_l}{L_l} \left(1 + \frac{\tilde{r}_l}{R_l}\right) \left(1 - \frac{\tilde{l}_l}{L_l}\right) + j\omega, \quad (3.53)$$

$$\cong -\frac{R_l}{L_l} \left(1 + \frac{\tilde{r}_l}{R_l} - \frac{\tilde{l}_l}{L_l}\right) + j\omega. \quad (3.54)$$

Also, the first term of the right-hand side of the last row of Eq. (3.51) can be approximated as

$$(M + \tilde{m})(I_{if} + \tilde{i}_{if}) \cong M I_{if} + I_{if} \tilde{m} + M \tilde{i}_{if}. \quad (3.55)$$

Applying this linearization approach to all the elements of Eq. (3.51) and noting that the derivative of the nominal quantities ($\frac{dI_{lf}}{dt}$, $\frac{dI_{lf}}{dt}$...) are zero, the resulting approximate equation can be represented in general form as

$$0 + \dot{\tilde{\mathbf{x}}}_{rr} = \mathbf{A}_{ss}\mathbf{X}_{rr} + \mathbf{U}_{rr} + \mathbf{A}_{s\tilde{s}}\tilde{\mathbf{x}}_{rr} + \mathbf{A}_m\mathbf{X}_{rr}\tilde{m} + \mathbf{A}_{ll}\mathbf{X}_{rr}\tilde{l}_l + \mathbf{A}_{rl}\mathbf{X}_{rr}\tilde{r}_l + \mathbf{A}_{dc}\tilde{v}_{dc}, \quad (3.56)$$

and,

$$\mathbf{A}_{dc} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L_s} & 0 \end{bmatrix}^T. \quad (3.61)$$

Equation (3.56) is the general linearized model of the system in the rotating frame of reference. It is used to obtain the low-frequency analytical models for the steady-state and dynamic analysis of the three-phase UPS system.

3.5 Steady-State Model and Analysis

The low-frequency steady-state model of the three-phase UPS system is obtained by setting all the perturbations in Eq. (3.56) (i.e. \tilde{m} , \tilde{r}_i , \tilde{l}_i , \tilde{v}_{dc} , $\tilde{\mathbf{x}}_{rr}$, $\dot{\tilde{\mathbf{x}}}_{rr}$) to zero. Equation (3.56) reduces to

$$\mathbf{A}_{ss} \mathbf{X}_{rr} + \mathbf{U}_{rr} = 0, \quad (3.62)$$

or,

$$\begin{bmatrix} -\frac{R_l}{L_f} + j\omega & 0 & -\frac{1}{L_f} & 0 & 0 & 0 & 0 & \frac{\sqrt{3}M}{4L_f} \\ 0 & -\frac{R_l}{L_l} + j\omega & \frac{1}{L_l} & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_f} & -\frac{1}{C_f} & j\omega & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_l}{L_f} - j\omega & 0 & -\frac{1}{L_f} & 0 & \frac{\sqrt{3}M}{4L_f} \\ 0 & 0 & 0 & 0 & -\frac{R_l}{L_l} - j\omega & \frac{1}{L_l} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_f} & -\frac{1}{C_f} & -j\omega & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{\sqrt{3}M}{4L_f} \\ -\frac{\sqrt{3}M}{4C_d} & 0 & 0 & -\frac{\sqrt{3}M}{4C_d} & 0 & 0 & \frac{1}{C_d} & 0 \end{bmatrix} \begin{bmatrix} I_{iF} \\ I_{lF} \\ V_{cF} \\ I_{iB} \\ I_{lB} \\ V_{lB} \\ I_{is} \\ V_d \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \frac{V_{dc}}{L_s} \\ 0 \end{bmatrix} = 0. \quad (3.63)$$

The steady-state variables in the rotating frame of reference are obtained from Eq. (3.63)

as

$$\mathbf{X}_{rr} = -(\mathbf{A}_{ss})^{-1} \mathbf{U}_{rr}. \quad (3.64)$$

Assuming that the resistances associated with the filter inductors are sufficiently small such that they have a negligible effect on the steady-state variables of the system, the steady-state variables can be approximated by setting R_s , and R_f to zero in Eq. (3.64). The approximate steady-state variables are given by

$$\tilde{I}_{iF} \cong \frac{K(R_i + j(R_i^2(\frac{X_{Ll}}{X_{Cf}^2} - \frac{1}{X_{Cf}}) + X_l(1 + \frac{X_l X_{Ll}}{X_{Cf}^2} - \frac{X_l}{X_{Cf}} - \frac{2X_{Ll}}{X_{Cf}}) + X_{Lf}))}{8((R_l - \frac{R_l X_{Ll}}{X_{Cf}})^2 + (X_{Lf} + X_l - \frac{X_{Ll} X_l}{X_{Cf}})^2)}, \quad (3.65)$$

$$\tilde{I}_{iB} \cong \frac{K(\tilde{R}_l - j(R_l^2(\frac{X_{Ll}}{X_{Cf}^2} - \frac{1}{X_{Cf}}) + X_l(1 + \frac{X_l X_{Ll}}{X_{Cf}^2} - \frac{X_l}{X_{Cf}} - \frac{2X_{Ll}}{X_{Cf}}) + X_{Lf}))}{8((R_l - \frac{R_l X_{Ll}}{X_{Cf}})^2 + (X_{Lf} + X_l - \frac{X_{Ll} X_l}{X_{Cf}})^2)}, \quad (3.66)$$

$$\tilde{I}_{lF} \cong \frac{K(R_l - \frac{R_l X_{Ll}}{X_{Cf}} + j(X_{Lf} + X_l - \frac{X_{Ll} X_l}{X_{Cf}}))}{8((R_l - \frac{R_l X_{Ll}}{X_{Cf}})^2 + (X_{Lf} + X_l - \frac{X_{Ll} X_l}{X_{Cf}})^2)}, \quad (3.67)$$

$$\tilde{I}_{lB} \cong \frac{K(R_l - \frac{R_l X_{Ll}}{X_{Cf}} - j(X_{Lf} + X_l - \frac{X_{Ll} X_l}{X_{Cf}}))}{8((R_l - \frac{R_l X_{Ll}}{X_{Cf}})^2 + (X_{Lf} + X_l - \frac{X_{Ll} X_l}{X_{Cf}})^2)}, \quad (3.68)$$

$$\tilde{V}_{cF} \cong \frac{K(R_i^2 + X_l^2 + X_l X_{Lf} - \frac{X_{Ll}}{X_{Cf}}(R_i^2 + X_l^2) + j R_l X_{Lf})}{8((R_l - \frac{R_l X_{Ll}}{X_{Cf}})^2 + (X_{Lf} + X_l - \frac{X_{Ll} X_l}{X_{Cf}})^2)}, \quad (3.69)$$

$$\tilde{V}_{cB} \cong \frac{K(R_i^2 + X_l^2 + X_l X_{Lf} - \frac{X_{Ll}}{X_{Cf}}(R_i^2 + X_l^2) - j R_l X_{Lf})}{8((R_l - \frac{R_l X_{Ll}}{X_{Cf}})^2 + (X_{Lf} + X_l - \frac{X_{Ll} X_l}{X_{Cf}})^2)}, \quad (3.70)$$

$$I_s \cong \frac{3 M^2 \tilde{V}_{dc} R_l}{(R_l - \frac{R_l X_{Ll}}{X_{Cf}})^2 + (X_{Lf} + X_l - \frac{X_{Ll} X_l}{X_{Cf}})^2}, \quad (3.71)$$

$$V_d \cong V_{dc}, \quad (3.72)$$

where

$$K = 2\sqrt{3} M V_{dc}, \quad (3.73)$$

and the X's represent the reactances at the angular frequency of the modulating signal.

In contrast to the numerical solution approach, Eqs. (3.65) to (3.72) give the closed-form solution of the low-frequency components of the circuit variables in terms of the circuit parameters, the input DC voltage, and the modulation index. Equation (3.71) can be used to design the input DC filter inductor since most of the high frequency ripples reflected by the inverter switching on the DC side will pass through the capacitor on the DC side of the inverter.

The system steady-state variables are not only used to determine the ratings of the power filter and the switching devices, they represent the nominal operating point for determining the dynamic response of the system.

3.6 Small-Signal Dynamic Model and Analysis

The small-signal dynamic model of the system is obtained from the general linearized model of Eq. (3.56) by setting all the terms with steady-state variables to zero. The resulting equation is obtained as

$$\dot{\tilde{\mathbf{x}}_{rr}} = \mathbf{A}_{ss} \tilde{\mathbf{x}}_{rr} + \mathbf{A}_m \mathbf{X}_{rr} \tilde{m} + \mathbf{A}_{li} \mathbf{X}_{rr} \tilde{l}_l + \mathbf{A}_{rl} \mathbf{X}_{rr} \tilde{r}_l + \mathbf{A}_{dc} \tilde{v}_{dc}. \quad (3.74)$$

The second term of Eq. (3.74) accounts for the effects of the small-signal variations in the control signal. Similarly, the third and fourth terms represent the effect of the variation in the load, while the fifth term accounts for the small variation in the DC input voltage. Thus, Eq. (3.74) gives the relationship between the incremental changes in the system state variables ($\tilde{\mathbf{x}}_{rr}$) due to incremental changes in the control signal, the load, and the input DC voltage.

Since Eq. (3.74) is linear, the superposition theorem can be applied to examine the dynamic response of the system to any of the above-mentioned disturbances. For example, the small-signal dynamic model of the system due to small variation in the control signal can be obtained from Eq. (3.74) by substituting $\tilde{l}_l = \tilde{r}_l = \tilde{v}_{dc} = 0$. The resultant small-signal AC model is given by

$$\dot{\tilde{\mathbf{x}}}_{rr} = \mathbf{A}_{ss} \tilde{\mathbf{x}}_{rr} + \mathbf{A}_m \mathbf{X}_{rr} \tilde{m}, \quad (3.75)$$

which on substituting for \mathbf{A}_{ss} , \mathbf{A}_m , and \mathbf{X}_{rr} from Eqs. (3.57), (3.58), and (3.64) can be rewritten as

$$\begin{bmatrix} \dot{\tilde{i}_{iF}} \\ \dot{\tilde{i}_{lF}} \\ \dot{\tilde{v}_{cF}} \\ \dot{\tilde{i}_{iB}} \\ \dot{\tilde{i}_{lB}} \\ \dot{\tilde{v}_{cB}} \\ \dot{\tilde{i}_s} \\ \dot{\tilde{v}_d} \end{bmatrix} = \begin{bmatrix} -\frac{R_l}{L_f} + j\omega & 0 & -\frac{1}{L_f} & 0 & 0 & 0 \\ 0 & -\frac{R_l}{L_l} + j\omega & \frac{1}{L_l} & 0 & 0 & 0 \\ \frac{1}{C_f} & -\frac{1}{C_f} & +j\omega & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_l}{L_f} - j\omega & 0 & -\frac{1}{L_f} \\ 0 & 0 & 0 & 0 & -\frac{R_l}{L_l} - j\omega & \frac{1}{L_l} \\ 0 & 0 & 0 & \frac{1}{C_f} & -\frac{1}{C_f} & -j\omega \\ 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{\sqrt{3}M}{4C_d} & 0 & 0 & -\frac{\sqrt{3}M}{4C_d} & 0 & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_{iF} \\ \tilde{i}_{lF} \\ \tilde{v}_{cF} \\ \tilde{i}_{iB} \\ \tilde{i}_{lB} \\ \tilde{v}_{cB} \\ \tilde{i}_s \\ \tilde{v}_d \end{bmatrix} + \begin{bmatrix} \frac{\sqrt{3}V_d}{4L_f} \\ 0 \\ 0 \\ \frac{\sqrt{3}V_d}{4L_f} \\ 0 \\ 0 \\ 0 \\ -\frac{\sqrt{3}}{4C_d}(I_{iF} + I_{iB}) \end{bmatrix} \tilde{m}. \quad (3.76)$$

The transfer function of the incremental variation in the control to the incremental change in the state variables is obtained by taking the Laplace transform of Eq. (3.75) and rearranging the resulting expression to give

$$\frac{\tilde{\mathbf{x}}_{rr}(s)}{\tilde{m}(s)} = (s\mathbf{I} - \mathbf{A}_{ss})^{-1} \mathbf{A}_m \mathbf{X}_{rr}, \quad (3.77)$$

where \mathbf{I} is the identity matrix and s is the Laplace operator.

Equation (3.77) shows that the location of the system poles and zeros in the s -plane are dependent on the steady-state operating point of the system state variables, the system parameters and the nominal value of the modulation index, M .

The magnitude of a generic state variable, y , in the rotating frame of reference is obtained from its forward and backward component using the general relationship [112]

$$|y| = \frac{2}{\sqrt{3}} \sqrt{y_F y_B}. \quad (3.78)$$

The amplitude of the capacitor voltage, v_c , is obtained in terms of its forward and backward components by replacing the forward and backward components of the generic variable y in Eq. (3.78) by the corresponding component of the capacitor voltage v_c , as

$$v_c = \frac{2}{\sqrt{3}} \sqrt{v_{cF} v_{cB}}, \quad (3.79)$$

where the variables v_c , v_{cF} , and v_{cB} are represented by their small-signal variations around their nominal operating point as

$$v_c = V_c + \tilde{v}_c, \quad (3.80)$$

$$v_{cF} = V_{cF} + \tilde{v}_{cF}, \quad (3.81)$$

$$v_{cB} = V_{cB} + \tilde{v}_{cB}. \quad (3.82)$$

Substituting Eqs. (3.80) to (3.82) into Eq. (3.79), and obtaining the first-order approximation of Eq. (3.79) using Taylor's expansion gives

$$V_c + \tilde{v}_c = \frac{2}{\sqrt{3}} (\sqrt{V_{cF} V_{cB}} + \tilde{v}_{cF} \frac{\partial v_c}{\partial v_{cF}} \Big|_{v_{cF}=V_{cF}, v_{cB}=V_{cB}} + \tilde{v}_{cB} \frac{\partial v_c}{\partial v_{cB}} \Big|_{v_{cF}=V_{cF}, v_{cB}=V_{cB}}). \quad (3.83)$$

The incremental variation in the amplitude of the capacitor voltage in terms of the incremental change of its forward and backward components is obtained from Eq. (3.83)

as

$$\tilde{v}_c = \frac{1}{\sqrt{3}} \left(\sqrt{\frac{V_{cB}}{V_{cF}}} \tilde{v}_{cF} + \sqrt{\frac{V_{cF}}{V_{cB}}} \tilde{v}_{cB} \right). \quad (3.84)$$

The transfer function of the incremental changes in the control to the amplitude of the capacitor voltage is obtained as

$$G_{vc}(s) = \frac{\tilde{v}_c(s)}{\tilde{m}(s)} = \frac{1}{\sqrt{3}} \left(\sqrt{\frac{V_{cB}}{V_{cF}}} \frac{\tilde{v}_{cF}(s)}{\tilde{m}(s)} + \sqrt{\frac{V_{cF}}{V_{cB}}} \frac{\tilde{v}_{cB}(s)}{\tilde{m}(s)} \right). \quad (3.85)$$

Equation (3.85) shows that the transfer function of the incremental changes of control to the amplitude of the capacitor voltage is composed of the transfer function of incremental changes of control to both the forward and backward components of the capacitor voltage. The values for V_{cF} and V_{cB} are obtained from Eq. (3.69) and Eq. (3.70) respectively, and are expressed as:

$$V_{cF} = |V_{cF}| e^{j\phi_{vc}}, \quad (3.86)$$

$$V_{cB} = |V_{cB}| e^{-j\phi_{vc}}, \quad (3.87)$$

where the phase angle ϕ_{vc} is defined by

$$\phi_{vc} = \tan^{-1} \frac{R_l X_{lf}}{R_l^2 + X_l^2 + X_l X_{lf} - \frac{X_{lf}}{X_{cf}} (R_l^2 + X_l^2)}. \quad (3.88)$$

Substituting Eqs. (3.86) and (3.87) into (3.85) gives

$$G_{vc}(s) = \frac{1}{\sqrt{3}} \left(e^{-j\phi_{vc}} \frac{\tilde{v}_{cF}(s)}{\tilde{m}(s)} + e^{j\phi_{vc}} \frac{\tilde{v}_{cB}(s)}{\tilde{m}(s)} \right). \quad (3.89)$$

The transfer functions $\frac{\tilde{v}_{cF}(s)}{\tilde{m}(s)}$ and $\frac{\tilde{v}_{cB}(s)}{\tilde{m}(s)}$ are obtained from the third and sixth rows of Eq. (3.77). Due to the complexity of the analytical expression of Eq. (3.89), numerical values of the system parameters are used to obtain the transfer function $\frac{\tilde{v}_c(s)}{\tilde{m}(s)}$.

The open-loop transfer function is expressed in the form

$$\frac{\tilde{v}_c(s)}{\tilde{m}(s)} = G_{vc}(s) = \frac{G_{vc(num)}(s)}{G_{vc(den)}(s)}, \quad (3.90)$$

where $G_{vc(num)}(s)$ and $G_{vc(den)}(s)$ can be written in the form

$$G_{vc(num)}(s) = k_1 ((s + \alpha_{z1})^2 + \omega_{z1}^2) ((s + \alpha_{z3})^2 + \omega_{z3}^2) \times ((s + \alpha_{z5})^2 + \omega_{z5}^2), \quad (3.91)$$

$$G_{vc(den)}(s) = ((s + \alpha_{p1})^2 + \omega_{p1}^2) ((s + \alpha_{p3})^2 + \omega_{p3}^2) \times ((s + \alpha_{p5})^2 + \omega_{p5}^2) ((s + \alpha_{p7})^2 + \omega_{p7}^2). \quad (3.92)$$

Equation (3.92) shows that the incremental dynamics of the capacitor voltage due to incremental changes in the modulation index in the three-phase UPS system is described by an eighth-order transfer function. Matlab, [113], was used to determine the location of the system poles and zeros for the system parameters:

$$\begin{array}{lll} L_f = 5.0 \text{ mH}, & C_f = 100 \text{ } \mu\text{F}, & V_{dc} = 160 \text{ volts}, \\ L_s = 10 \text{ mH}, & C_d = 5000 \text{ } \mu\text{F}, & M = 0.9. \end{array}$$

Figure 3.2 shows the pole-zero map of the transfer function of Eq. (3.90) for a load of $z_l = 10 \text{ } \Omega$ at 0.7 power factor lagging. The figure shows that one of the system complex pole pairs ($p_1 - p_2$) is located in very close proximity to a complex zero pair ($z_1 - z_2$). The effects of these complex pole-zero pairs cancel and result in negligible contribution to the overall transfer function of the incremental changes in the capacitor voltage. Also, the complex pole-pairs $p_3 - p_4$ and $p_7 - p_8$ are placed relatively close to the complex zero pairs $z_3 - z_4$ and $z_5 - z_6$ respectively. The effect of this complex pole-zero arrangement on the overall dynamic behaviour of the system cancel out. As a result, the transfer function can be reduced to a second-order system

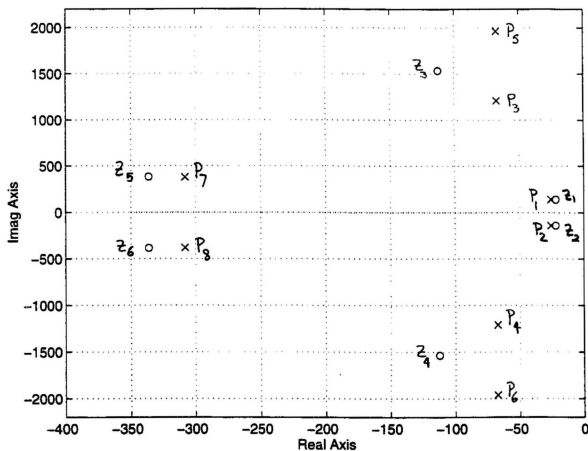


Figure 3.2: Pole-zero map of the open-loop transfer function of the capacitor voltage for $z_l = 10.0 \Omega$ at 0.7 power factor lagging load

as

$$G_{ver}(s) = \frac{k_2}{((s + \alpha_{ps})^2 + \omega_{ps}^2)}, \quad (3.93)$$

where the subscript r denotes the reduced-order transfer function.

The gain k_2 in Eq. (3.93) is determined such that the final value of the system response to a step input is the same for the full-order transfer function (Eq. (3.90)) and the reduced-order transfer function. Using the final-value theorem, k_2 is determined as

$$k_2 = k_1 \frac{\omega_{z1n}^2 \omega_{z3n}^2 \omega_{z5n}^2}{\omega_{p1n}^2 \omega_{p3n}^2 \omega_{p7n}^2}, \quad (3.94)$$

where ω_{z1n} , ω_{z3n} , ω_{z5n} , ω_{p1n} , ω_{p3n} , and ω_{p7n} are the natural frequencies of the complex zeros z_1 to z_6 , and poles p_1 to p_4 and p_6 – p_7 respectively. Equation (3.93) shows that the behaviour of the incremental change in the capacitor voltage due to incremental changes in the control signal is governed mainly by the lightly damped dominant poles, p_5 and p_6 .

Figure 3.3 shows the pole-zero map of the transfer function for a load of $z_l = 10 \Omega$ at unity power factor. The figure shows that all the system poles and zeros have been shifted farther into the left-hand side of the s -plane indicating higher damping ratio. This has the effect of faster damping of the system oscillations. The figure shows pole-zero cancellation carried out for the 0.7 power factor lagging load is valid under various load variation.

Figure 3.4 shows the Bode diagram of the open-loop transfer function of the capacitor voltage along with its experimental verification. The figure was obtained for the following system parameters:

$$\begin{array}{llll} V_{dc} = 140 \text{ volts,} & L_s = 10 \text{ mH,} & C_d = 5000 \mu\text{F,} & L_f = 5.0 \text{ mH,} \\ C_f = 100 \mu\text{F,} & M = 0.9, & Z_l = 17.0 \Omega \text{ at } 0.75 \text{ pf lagging,} & F_s = 4.0 \text{ kHz.} \end{array}$$

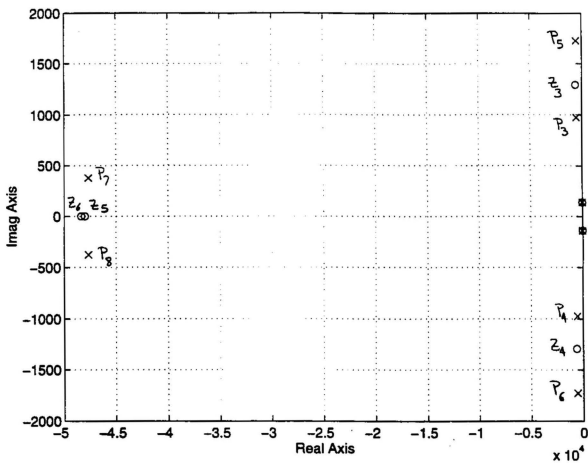


Figure 3.3: Pole-zero map of the open-loop transfer function of the capacitor voltage for $z_l = 10.0 \Omega$ at unity power factor load

The figure shows close agreement between the predicted and experimental results especially at low frequencies, and validates the analysis procedures presented. The discrepancy between the predicted and experimental results at high frequency is expected since the small-signal model becomes inaccurate at frequencies higher than half the switching frequency.

3.7 Incremental Dynamics in the Three-Phase UPS System

In Chapter Two it was shown that using the capacitor current and voltage in an inner and outer control loops results in stable and improved performance of the single-phase UPS system. In this section, the incremental dynamics of the capacitor voltage and current based on the forward-backward transformation are developed and used to examine the dynamic behaviour of the three-phase UPS system.

3.7.1 Incremental Dynamics of the Capacitor Voltage

The root-locus method is employed to examine the stability of the closed-loop operation of the system. The root-locus plots of the incremental dependence of the capacitor voltage on the incremental variation in the modulating signal for 10% perturbation in the control signal (\tilde{m}) around the nominal value, M , are shown in Figs. 3.5 and 3.6 for two sets of load parameters. The figures show that by simply closing the loop around the capacitor voltage, the dominant complex pole-pairs move parallel to the imaginary axis of the s-plane as the modulation index changes. However, this excursion is periodic, and depends on the system parameters and the nominal value of the modulation index. This results in a lightly damped oscillating load voltage.

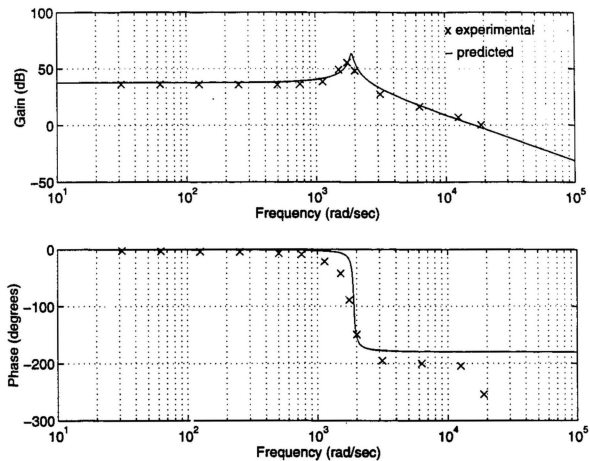


Figure 3.4: Experimental verification of the frequency response of the open-loop transfer function of the capacitor voltage for $Z_l=17.0 \, \Omega$ at 0.75 power factor lagging load

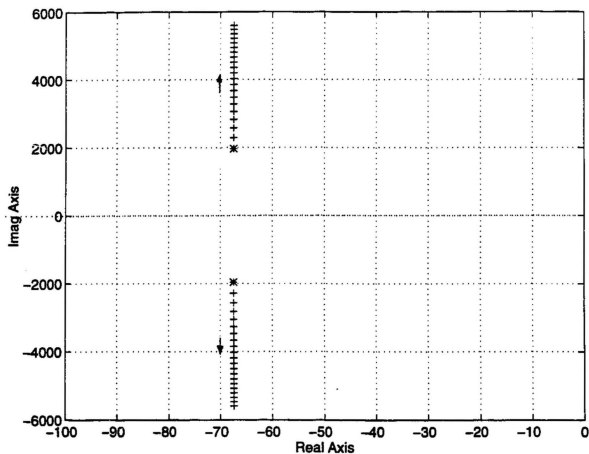


Figure 3.5: Root locus of the incremental change of the capacitor voltage due to incremental variation in the modulating signal for $Z_l = 10.0\Omega$ at 0.7 power factor lagging load

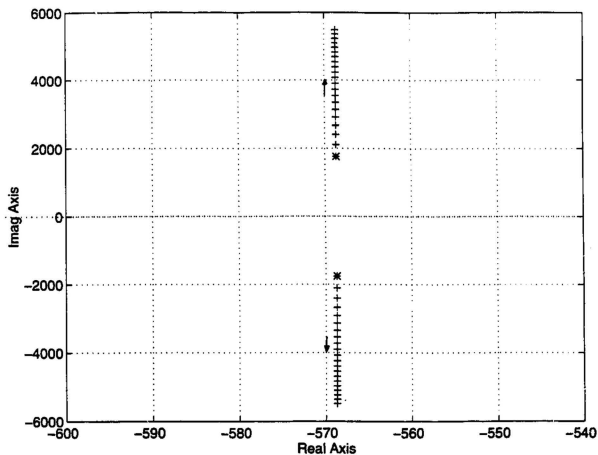


Figure 3.6: Root locus of the incremental change of the capacitor voltage due to incremental variation in the modulating signal for $Z_l = 10.0\Omega$ at unity power factor load

The excursion in the system frequency is 2500 rad/sec.

In the case of unity power factor loads, Fig. 3.6, shows that the system poles have been shifted farther into the left-half of the s-plane. This has the effect of faster damping of the load voltage oscillations.

It is worth mentioning that the system complex conjugate poles periodically move parallel to the imaginary axis of the s-plane. In other words, the locations of the poles in the s-plane of the system under investigation are not only dependent on the system parameters and the nominal operating point of the modulation index, but they are also time-varying.

3.7.2 Incremental Dynamics of the Capacitor Current

The transfer function of the incremental changes in the amplitude of the capacitor current due to incremental variation in the modulation can be derived from Eq. (3.93)

as

$$\frac{\tilde{i}_{cr}(s)}{\tilde{m}(s)} = G_{icr}(s) = C_f s G_{vcr}(s). \quad (3.95)$$

The pole-zero map of Eq. (3.95) for $Z_l = 10.0 \Omega$ at 0.7 power factor lagging loads is shown in Fig. 3.7. The figure shows that the pole-zero map of the incremental changes in the capacitor current is the same as that of the capacitor voltage with the addition of a zero at the origin.

Figures 3.8 and 3.9 show the root locus of the incremental changes in the capacitor current for 10% perturbation in the control signal. The figures show that using the capacitor current as the feedback variable in the three-phase UPS system guarantees stable operation of the system for a wide range of system parameters. The incremental dynamics in the three-phase UPS system exhibit the same characteristics as the single-

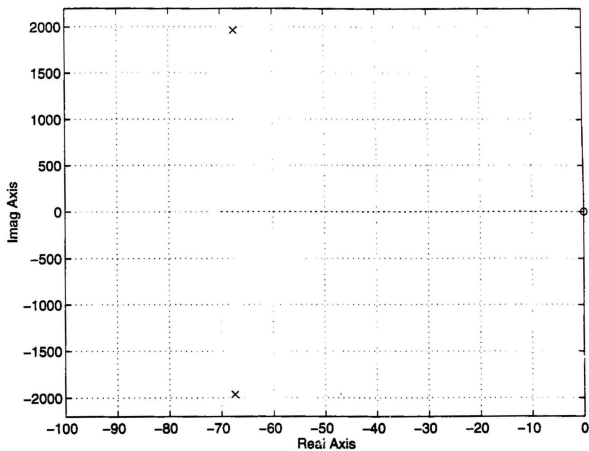


Figure 3.7: Pole-zero map of $G_{tcr}(s)$ for $Z_l = 10.0\ \Omega$ at 0.7 power factor lagging load

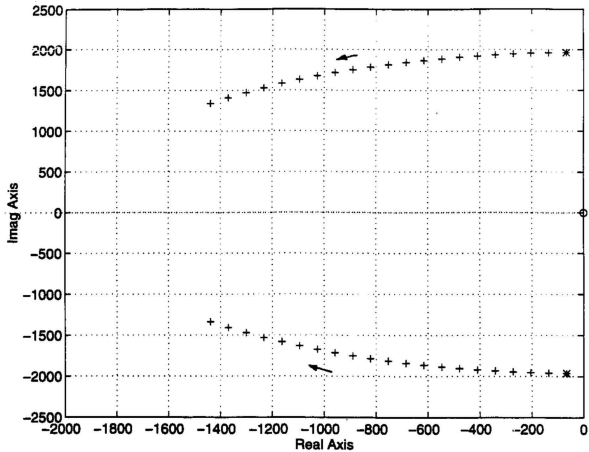


Figure 3.8: Root locus of the incremental change in the capacitor current due to incremental variation in the modulating signal at $Z_l = 10.0\Omega$ at 0.7 power factor lagging load

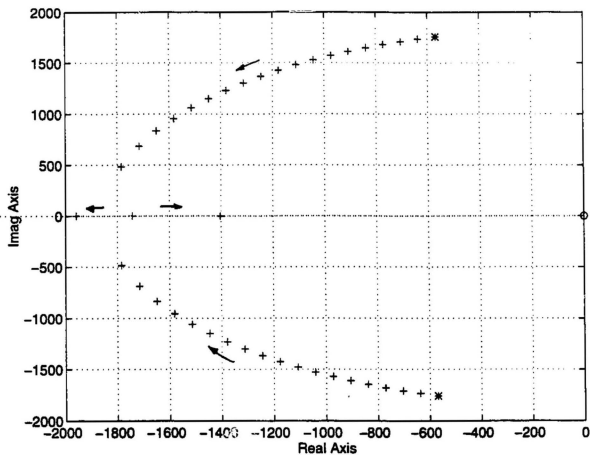


Figure 3.9: Root locus of the incremental change in the capacitor current due to incremental variation in the modulating signal for $Z_l = 10.0\Omega$ at unity power factor load

phase UPS. Hence, the same procedures can be used to select the appropriate values of the proportional controllers.

3.8 Computer Simulation of the Three-Phase UPS System

The three-phase UPS system employing the proposed control strategy is shown in Fig. 3.10. Computer simulation of the operation of this system was carried out to obtain various waveforms in the system for the following parameters:

$$\begin{array}{llll} L_s = 10 \text{ mH}, & C_d = 5000 \text{ } \mu\text{F}, & L_f = 5.0 \text{ mH}, & C_f = 100 \text{ } \mu\text{F}, \\ V_{dc} = 140.0 \text{ Volts}, & Z_l = 17.0 \text{ } \Omega \text{ at } 0.75 \text{ pf lagging}, & & F_s = 4.0 \text{ kHz}, \\ k_{pc} = 2.0, & k_{pv} = 2.0. & & \end{array}$$

To reduce the in-rush current at the inverter output during the “cold” start of the UPS system, a time-varying gain in the outer voltage loop is used. The value of k_{pv} is set to ramp up from zero at start to its full value ($k_{pv}=2.0$) during the first cycle. Details of the electronic circuit to obtain this soft-start mechanism are provided in Appendix A.

Figure 3.11 shows the voltage of the input DC capacitor and the DC-source current. The simulation results give a DC capacitor voltage of 139.2 volts for a DC source voltage of 140.0 volts. The corresponding DC source current, i_s , (Fig. 3.11.ii) has a steady-state value of 1.68 Amperes. Substituting the values of the system parameters given above in Eq. (3.71), the steady-state model predicts a steady-state value of 1.60 Amperes. This confirms the validity of the theoretical model. Fig. 3.12 shows the three-level waveform of the inverter line-to-neutral voltage. Figure 3.13 shows the three-phase inverter output currents. The currents are balanced and sinusoidal with superimposed high-frequency switching ripples.

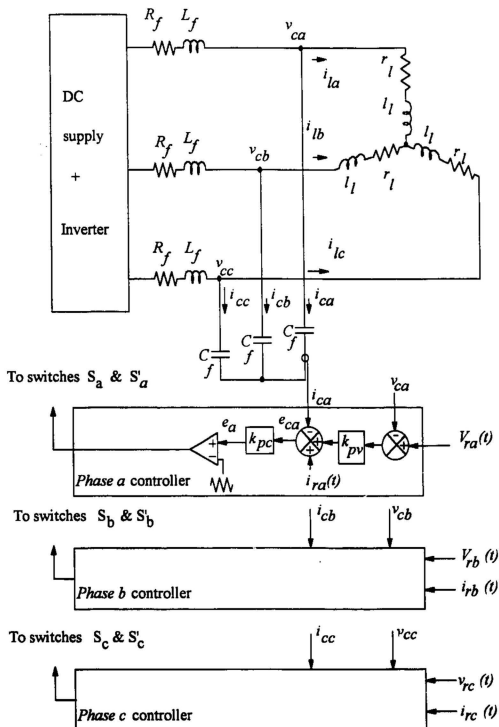


Figure 3.10: The proposed three-phase UPS system

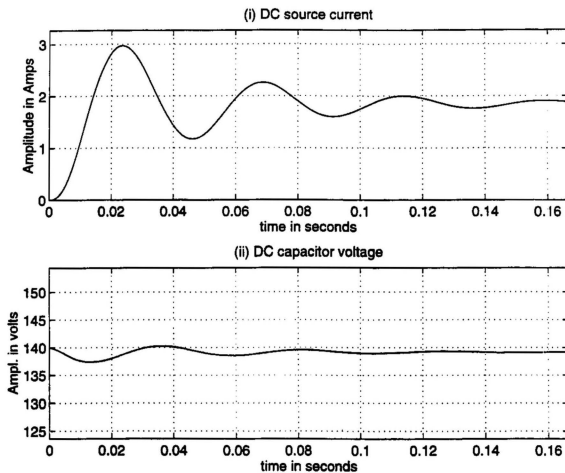


Figure 3.11: Simulation waveforms of the DC side quantities of the power inverter

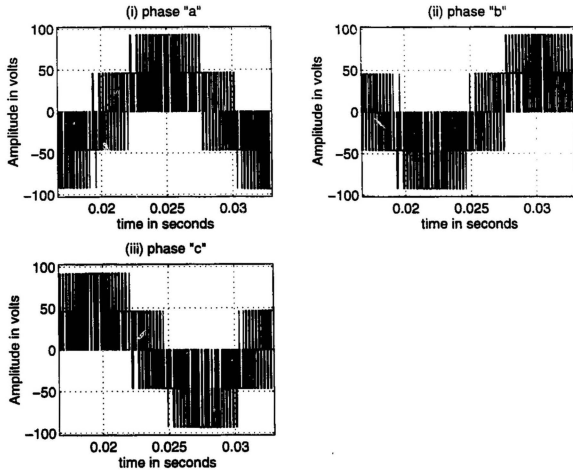


Figure 3.12: Simulation waveforms of the three-phase inverter output line-to-neutral voltage

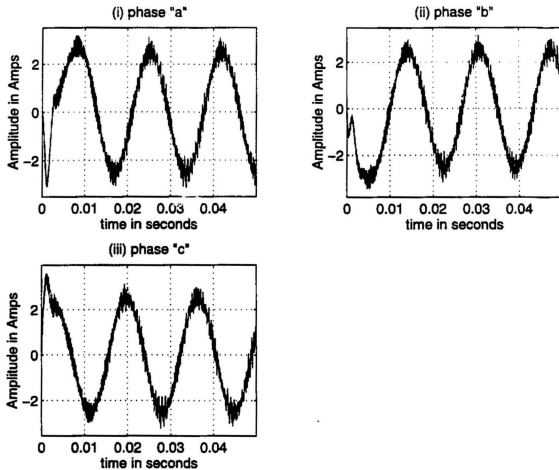


Figure 3.13: Simulation waveforms of the three-phase inverter output current

The three-phase line-to-neutral load (capacitor) voltage is depicted in Fig 3.14. The capacitor voltage has no DC offset and is nearly perfect sinusoid with a small steady-state error. The figure also shows that the system takes about one cycle (based on the reference signal frequency) to reach steady-state from “cold” start with the system fully loaded. Figure 3.15 shows the corresponding capacitor current.

3.9 Experimental Verification

An experimental module of the proposed three-phase UPS system shown in Fig. 3.10 was constructed in the laboratory. The input DC source was obtained from a readily available power supply which employed a three-phase half-bridge rectifier with a second-order filter at its output. An external DC capacitor was employed at the output of the DC power supply to ensure a stable DC voltage at the input of the inverter. To prevent shoot-through faults, a dead-time interval of 10 μ sec was introduced when switching from an upper to lower device or vice versa in the same inverter leg. The details of the control circuit used to generate the dead-time interval are provided in Appendix A.

Figure 3.16 shows the experimental waveforms of the three-phase line-to-neutral load voltage. The load voltage is nearly perfect sinusoid with a THD of 1.9%. Figure 3.17 shows the three-phase capacitor current waveforms. The current waveforms were measured using a clamp-on meter with a scaling factor of one milli-volt per one ampere output.

Figure 3.18 shows the transient response of the load voltage from “cold” start to full load with the system fully loaded. The figure shows that the system takes approximately one-cycle to reach steady state. The dynamic response of the system

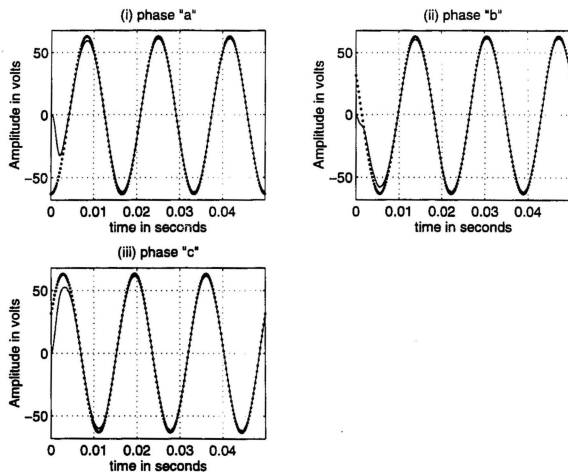


Figure 3.14: Simulation waveforms of the three-phase load voltages (line-to-neutral)

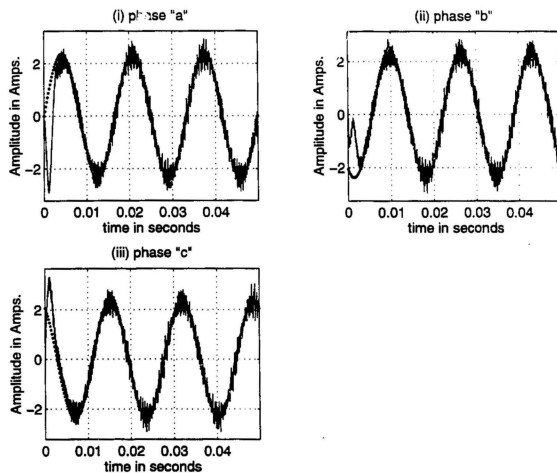
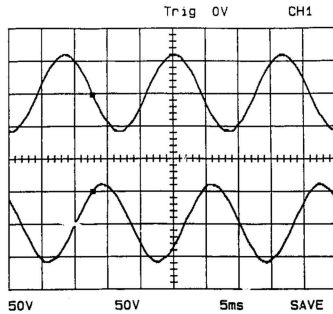
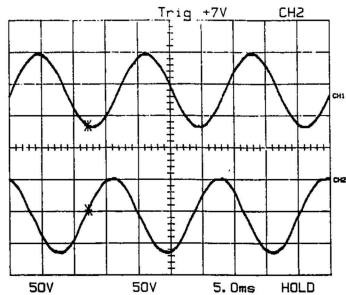


Figure 3.15: Simulation waveforms of the three-phase capacitor currents

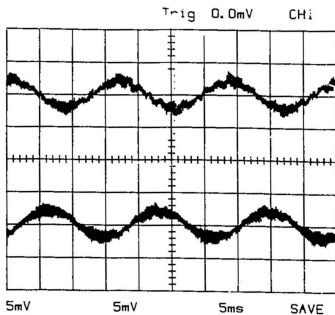


(i)

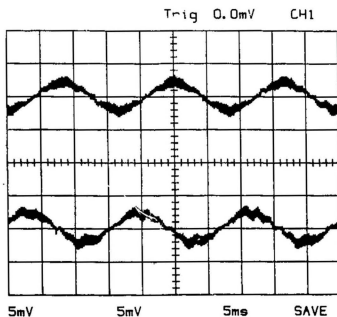


(ii)

Figure 3.16: Experimental waveforms of the load voltage (line-to-neutral): (i) upper trace: *phase a*, lower trace: *phase b*, (ii) upper trace: *phase a*, lower trace: *phase c*.

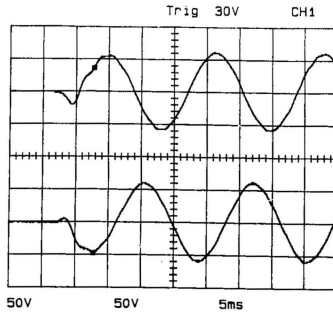


(i)

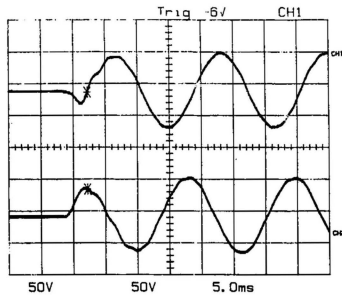


(ii)

Figure 3.17: Experimental waveforms of the capacitor currents: (i) upper trace: *phase a*, lower trace: *phase b*, (ii) upper trace: *phase a*, lower trace: *phase c*



(i)



(ii)

Figure 3.18: Experimental waveforms of transient response of the load voltage: (i) upper trace: *phase a*, lower trace: *phase b*, (ii) upper trace: *phase a*, lower trace: *phase c*

for 100% step change in the load is depicted in Fig. 3.19. The step change in load was carried out by connecting a three-phase bidirectional static switches between the load and the UPS system. Figure 3.19 shows that the sudden application of the load results in little effect on the capacitor voltage.

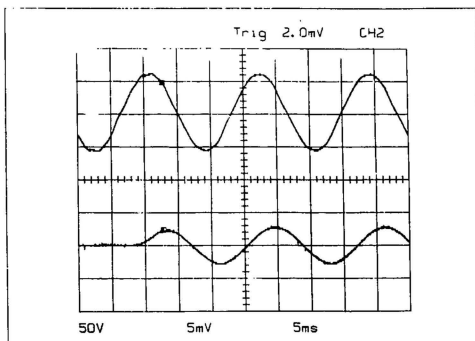


Figure 3.19: Experimental waveforms of transient response of the load voltage: upper trace: load voltage of *phase a*, lower trace: load current of *phase a*

Table 3.1 presents the peak values of the 60 Hz components of the AC quantities of the UPS system as measured from the practical circuit along with their predicted values obtained from Eqs. (3.65) to (3.70). The table shows that both the experimental and predicted values of the low-frequency model are in close agreement.

Table 3.1: Experimental verification of the steady-state values of the low-frequency model

	$Z_l=17.0 \Omega$ at 0.75 pf lagging		$Z_l=12.0 \Omega$ at unity pf lagging	
	Experimental	Predicted	Experimental	Predicted
I_i (Amps.)	2.38	2.46	5.32	5.45
V_c (volts)	57.78	59.80	57.39	59.69
I_c (Amps.)	2.07	2.24	2.16	2.25
I_l (Amps.)	3.38	3.51	4.82	4.97

3.10 Summary

The performance of the three-phase UPS system using the proposed control scheme was investigated. First, a general model of the three-phase UPS power circuit was developed with the input DC filter dynamics taken into account. An averaged low-frequency time-variant model was then derived from the general discontinuous model. In order to obtain analytical models to examine the steady-state and dynamic performance of the system, the low-frequency state-space model was transformed into the rotating frame of reference employing the forward-backward transformation. The result was a time-invariant non-linear model in the rotating frame of reference.

Steady-state and small-signal dynamic models were then derived using the per-

turbation and small-signal analysis technique. The model was used to examine the power circuit incremental dynamics. In particular, the transfer function of the incremental variation of the capacitor current due to incremental variation of the control signal was derived and used to assess the stability of the system. Using the pole-zero map of the capacitor current transfer function and the root-locus technique, it was shown that the proposed control scheme results in stable and successful operation of the three-phase UPS system.

Computer simulation and experimental verification of the proposed three-phase voltage-source UPS system were carried out. The results show that the proposed scheme offers excellent load-voltage regulation, fast dynamic response, and high-quality load voltage. The results confirm the analytical models and establish the feasibility of the control scheme for UPS applications.

Chapter 4

The Single-Phase Voltage-Source Utility Interactive System

This chapter deals with the application of the controller proposed in Chapter Two to utility interactive inverters. As indicated in the thesis objectives, one of the goals of this work is to develop a unified control scheme for both UPS and utility interactive applications. This chapter investigates the performance of a single-phase utility interactive system with the control scheme proposed in Chapter Two.

Following the analytical procedure outlined in Chapter Two, steady-state and small-signal dynamic models of the single-phase UIS are developed and used to describe the characteristics of the system over a wide range of operating conditions. Using the small-signal model, and the incremental dynamics analysis, it is shown that contrary to what intuition dictates, using the utility line current as the feedback variable results in unstable operation of the UIS. Consequently, the proposed control strategy, consisting of an inner capacitor current and outer capacitor voltage loops, not only results in stable operation of the system, but also provides an effective, albeit indirect, approach to shaping and controlling the utility line current.

Computer simulation and experimental verification of the operation of the single-

phase UIS feeding current at unity power factor and 90° leading into the utility voltage are presented to demonstrate the effectiveness of the proposed control scheme.

4.1 Low-Frequency Model of the Single-Phase Utility Interactive Inverter

Figure 4.1 shows the circuit diagram of the single-phase voltage-source utility in-

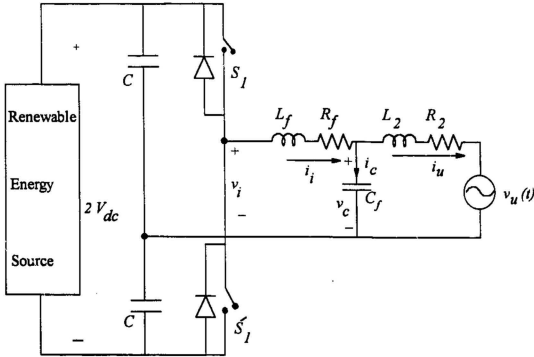


Figure 4.1: Power circuit of the utility interactive inverter

teractive system. It consists of a single-phase voltage-source half-bridge inverter, a second-order ($L_f - C_f$) filter and the utility network. The $L_f - C_f$ filter ensures

that both the capacitor voltage, v_c , and the utility line current are sinusoidal. The filter also makes the system compatible with weak utility networks; it minimizes the voltage distortion across the equivalent AC impedance of the weak utility network, and ensures a high-quality waveform at the point of common coupling. The utility network is represented by the Thevenin circuit comprising the utility voltage v_u in series with $L_2 - R_2$, which includes the parameters of the isolation transformer.

The governing differential equation of the UIS is given in state-space representation as

$$\begin{bmatrix} \frac{di_i}{dt} \\ \frac{di_u}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & -\frac{R_2}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_i \\ i_u \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} & 0 \\ 0 & -\frac{1}{L_2} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} (2S_1^* - 1)v_{dc} \\ v_u(t) \end{bmatrix}, \quad (4.1)$$

where $S_1^* = 1$ when switch S_1 is ON (S_1' OFF) and $S_1^* = 0$ when S_1 is OFF (S_1' is ON).

The system behaviour at frequencies much lower than the inverter switching frequency can be studied using the low-frequency model. The low-frequency model is obtained from Eq. (4.1) by replacing S_1^* with its time-average, d_1 .

For a modulating signal of the form

$$m(t) = m \cos(\omega t + \gamma), \quad (4.2)$$

where γ is the phase angle measured with respect to the utility voltage, the duty cycle of switch S_1 is given by

$$d_1 = \frac{m(t) + 1}{2}. \quad (4.3)$$

Substituting d_1 for S_1^* in Eq. (4.1), the averaged time-continuous model can be written

as

$$\begin{bmatrix} \frac{di_i}{dt} \\ \frac{di_u}{dt} \\ \frac{dq_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & -\frac{R_u}{L_u} & \frac{1}{L_u} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_i \\ i_u \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{2L_f} & 0 \\ 0 & -\frac{1}{L_u} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} m(t)v_{dc} \\ v_u(t) \end{bmatrix}. \quad (4.4)$$

Equation (4.4) shows that for frequencies much lower than the inverter switching frequency, the inverter output voltage can be modeled as a controllable sinusoidal voltage source whose peak value is determined by the level of the DC voltage source and the modulation index:

4.1.1 Steady-State Analysis of the Low-Frequency Model

The steady-state circuit model of the UIS is shown in Fig. 4.2. The steady-state

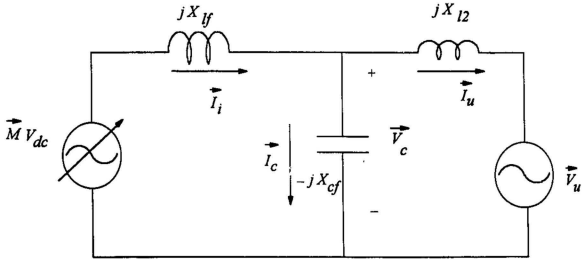


Figure 4.2: Low-frequency model of the UIS

variables can be obtained using phasor analysis. Assuming that the resistance associ-

ated with the inductors are negligibly small, the steady-state variables of the lossless model of the UIS can be written as

$$\tilde{I}_i = \frac{M V_{dc} (X_{l2} - X_{lf}) \angle \gamma + \frac{\pi}{2} - V_u X_{cf} \angle -\frac{\pi}{2}}{\sqrt{2} (X_{l2} X_{cf} + X_{lf} (X_{cf} - X_{l2}))}, \quad (4.5)$$

$$\tilde{V}_c = \frac{M V_{dc} \angle \gamma}{\sqrt{2}} - j \tilde{I}_i X_{lf}, \quad (4.6)$$

$$\tilde{I}_u = \frac{M V_{dc} X_{cf} \angle \gamma + \frac{\pi}{2} - V_u (X_{lf} - X_{cf}) \angle \frac{\pi}{2}}{\sqrt{2} (X_{l2} X_{cf} + X_{lf} (X_{cf} - X_{l2}))}. \quad (4.7)$$

where the X's are calculated at the frequency of the utility network.

4.1.2 Effect of the Filter Parameters on the Steady-State Operation of the UIS

Equation (4.7) shows that depending on the magnitude and phase of the inverter output voltage, both the magnitude and phase of the current injected into the utility network can be controlled. The characteristics of the UIS operating at two extreme power factors (i.e., \tilde{I}_u in phase and 90° leading) with respect to the utility voltage are examined.

Figure 4.3 shows the phasor diagram of the steady-state operation of the UIS for the two operating conditions. In order to operate the UIS successfully at any power factor ranging from unity to zero leading, the UIS should be capable of providing the required voltage magnitude and phase angle of the fundamental component of the inverter output V_{i1} . For a maximum modulation index $M = 1$, the peak value of the fundamental component of the inverter output voltage is equal to the input DC voltage level.

Figure 4.3.a shows that for zero-leading power factor operation, the required magnitude of V_i is less than that of the utility voltage. Higher values of either L_f or L_2 or

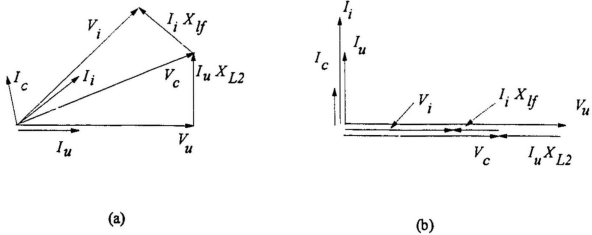


Figure 4.3: Phasor diagram of the steady-state operation of the UIS: a) unity power factor operation, b) zero-leading power factor operation.

both, decreases the required magnitude of the fundamental component of the inverter output voltage. In other words, depending on the values of the filter parameters and the voltage level available at the output of the renewable energy source, this system can operate at zero-leading power factor with input DC voltage much less than the magnitude of the utility voltage.

Figure 4.3.b shows the phasor diagram of the UIS when the system is operating at unity power factor. Depending on the value of the filter parameters, the required magnitude of V_i could be greater, equal to, or less than the magnitude of the utility voltage. Figure 4.3.b also shows that increasing the value of the filter inductor results in an increase in the required magnitude of the fundamental component of the inverter output voltage and vice versa.

Figure 4.4 shows the effect of the filter shunt capacitor on the magnitude of the

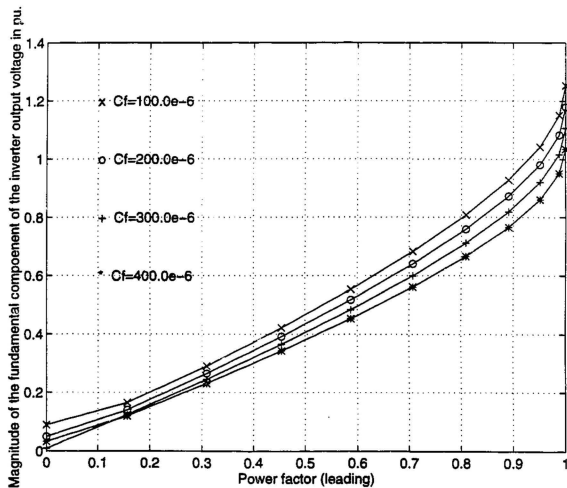


Figure 4.4: Relationship between the required magnitude of the fundamental component of the inverter output voltage and the power factor for various values of filter shunt capacitor.

fundamental component of the inverter output voltage for a wide range of power factor operation. The figure was obtained for 10 KVA UIS feeding current into a power grid at 208 volts, with $L_f = L_2 = 5.0$ mH. The magnitude of the utility voltage and current fed into the power grid were taken as base voltage and current respectively.

Figure 4.4 shows that for given values of the filter inductors, smaller values of the filter shunt capacitor necessitate higher magnitude of the fundamental of the inverter output voltage and hence higher DC level.

In summary, it can be concluded that for continuous control of the angle at which the utility current is injected into the power grid, the filter parameters should be chosen for the worst-case condition; i.e. unity power factor operation.

4.2 Small-Signal Model of the UIS

The main purpose of a utility interactive system is to produce a sinusoidal line current whose amplitude and phase angle with respect to voltage of the utility network are controllable. Intuitively, the output current of the UIS could be used as the feedback variable in the control circuit. The utility line current would be sensed and compared with its reference sinusoidal waveform. The output of the comparator would then be used to control the inverter switching devices such that the error between the actual utility line current and its reference waveform is minimized. With the aid of the small-signal model of the UIS, it is shown that employing the utility line current as the feedback variable results in unstable feedback operation of the UIS.

The small-signal model of the single-phase UIS is derived from its averaged time-continuous model, Eq. (4.4), using perturbation and small-signal approximation technique. This model is used to examine the incremental dynamics of the state variables

of the power circuit. The system state variables are perturbed around their nominal operating point as

$$i_i(t) = I_i(t) + \tilde{i}_i, \quad (4.8)$$

$$i_u(t) = I_u(t) + \tilde{i}_u, \quad (4.9)$$

$$v_c(t) = V_c(t) + \tilde{v}_c. \quad (4.10)$$

For the controller,

$$m(t) = M(t) + \tilde{m}; \quad (4.11)$$

for the input,

$$v_{dc}(t) = V_{dc} + \tilde{v}_{dc}; \quad (4.12)$$

and for the load,

$$v_u(t) = V_u(t) + \tilde{v}_u(t). \quad (4.13)$$

Substituting Eqs. (4.8) to (4.13) into Eq. (4.4), and neglecting non-linear and higher-order terms, the small-signal linearized model is obtained as

$$\begin{bmatrix} \dot{\tilde{i}}_i \\ \dot{\tilde{i}}_u \\ \dot{\tilde{v}}_c \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & -\frac{R_2}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_i \\ \tilde{i}_u \\ \tilde{v}_c \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}\tilde{m}(t)}{L_f} \\ -\frac{\tilde{v}_u}{L_2} \\ 0 \end{bmatrix}. \quad (4.14)$$

The transfer function of the state variables of the power circuit due to incremental changes in the control signal is obtained from Eq. (4.14) by setting the load disturbance, \tilde{v}_u to zero. Taking the Laplace transform of Eq. (4.14), the transfer function of the incremental changes in the state variables due to incremental changes in the modulating signal is obtained as

$$\frac{\begin{bmatrix} \tilde{i}_i(s) \\ \tilde{i}_u(s) \\ \tilde{v}_c(s) \end{bmatrix}}{\tilde{m}(s)} = \frac{\begin{bmatrix} s^2 + \frac{R_2}{L_2}s + \frac{1}{L_2 C_f} \\ \frac{1}{L_2 C_f} \\ \frac{1}{C_f}(s + \frac{R_2}{L_2}) \end{bmatrix}}{s^3 + a_2 s^2 + a_1 s + a_0}, \quad (4.15)$$

where

$$a_2 = \frac{R_f}{L_f} + \frac{R_2}{L_2}, \quad (4.16)$$

$$a_1 = \frac{1}{L_f L_2} (R_f + R_2 + \frac{L_f L_2}{C_f}), \quad (4.17)$$

$$a_0 = \frac{R_f + R_2}{C_f L_f L_2}. \quad (4.18)$$

Since the incremental variations in the capacitor current are given by

$$\tilde{i}_c = \tilde{i}_i - \tilde{i}_u, \quad (4.19)$$

the transfer function of the capacitor current is given by

$$\frac{\tilde{i}_c(s)}{\tilde{m}(s)} = \frac{s(s + \frac{R_2}{L_2})}{s^3 + a_2 s^2 + a_1 s + a_0}. \quad (4.20)$$

4.2.1 Incremental Dynamics of the Power Circuit State Variables

The root locus of the incremental dynamics of various state variables of the power circuit due to incremental changes in the control signal is investigated in this section. The results of the investigation are used to confirm the applicability of the proposed control scheme to the UIS.

Figure 4.5.a shows the root locus of the incremental changes in the utility line current due to incremental variation in the control signal. The figure shows that simply closing the loop around the utility current results in moving the system complex conjugate poles to the right-hand side of the s-plane. This has the effect of causing a monotonous increase in the magnitude of the utility current, resulting in unstable operation of the UIS.

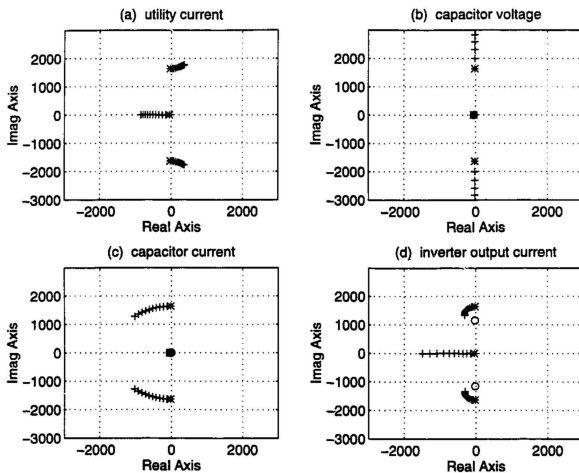


Figure 4.5: Root loci of the incremental changes of the power circuit state variables due to incremental variations in the modulating signal

Figure 4.5.c shows that selecting the capacitor current as the feedback variable would result in moving the system poles farther into the left-hand side of the s-plane, and hence stable closed-loop operation of the UIS system can be achieved.

4.2.2 Closed-Loop Operation of the UIS

Figure 4.6 shows the single-phase voltage-source UIS system with the capacitor current employed as the feedback variable in an inner current loop and the capacitor voltage in the outer voltage loop. For the UIS, the proposed control scheme provides an indirect approach to control the utility line current. Depending on the pre-calculated value of the power available from the renewable energy source and the active and reactive power to be injected into the power grid, both the magnitude and phase of the utility line current can be determined. The magnitude and phase of the capacitor voltage are then determined from the phasor relationship given in Fig. 4.3.

4.3 Computer Simulation of the UIS

The single-phase UIS shown in Fig. 4.6 is simulated to obtain various waveforms in the circuit. Closed-form solution of the state variables of the power circuit (Eq. (4.1)) was obtained using MAPLE. The following system parameters were used:

$$\begin{array}{lll} L_f=5.0 \text{ mH}, & C_f=340.0 \text{ } \mu\text{F}, & L_2=5.0 \text{ mH}, \\ F_s=4.0 \text{ kHz}, & k_{pc}=2.0, & k_{pu}=5.0. \end{array}$$

The simulation process was carried out from cold start (initial value of the state vector is zero) to full load. The power circuit was first operated at no-load (i.e. with the utility voltage disconnected). The no-load operation was sustained for approximately $\frac{1}{4}$ of a cycle to allow the capacitor voltage and current to follow their respective

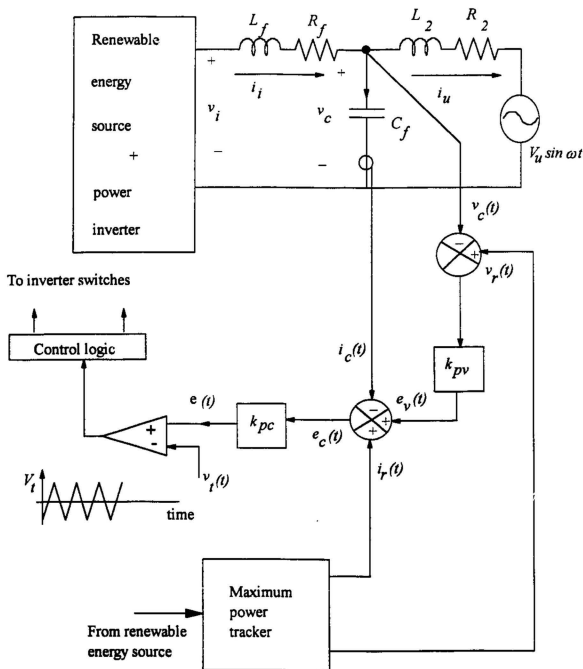


Figure 4.6: The proposed closed-loop single-phase voltage-source UIS

reference waveforms before interfacing the UIS with the utility network.

Figures 4.7 to 4.9 show the computer simulation results of various waveforms of the single-phase UIS for zero-leading power factor operation. Figure 4.7 shows that the capacitor voltage and current closely follow their respective reference waveforms (shown in dotted lines) after approximately one cycle from cold start of the UIS system. Figure 4.9 shows that the UIS generates sinusoidal steady-state output current once the utility interactive system is interfaced with the utility network. The steady-state error in the utility line current is negligibly small.

Figures 4.10 to 4.12 show the simulation results of various waveforms in the single phase UIS system for unity power factor operation. Figure 4.12 shows that the line current takes a longer time to reach its steady-state value than in the case of the zero-leading power factor operation. This is due to the fact that the UIS is interfaced with the utility voltage at an instant when the reference of the utility line current is at its peak while the actual current is zero.

4.4 Experimental Results

A prototype single-phase voltage-source UIS was constructed and used to demonstrate the feasibility of the proposed scheme. The renewable energy source was represented by a DC voltage source.

To successfully implement the system, the high-frequency carrier waveform is synchronized with the utility voltage using phase-locked loop circuit as a frequency multiplier. Hence, the inverter output switching frequency is in synchronism with the utility voltage. The block diagram for generating the high-frequency carrier waveform is described in Appendix A.

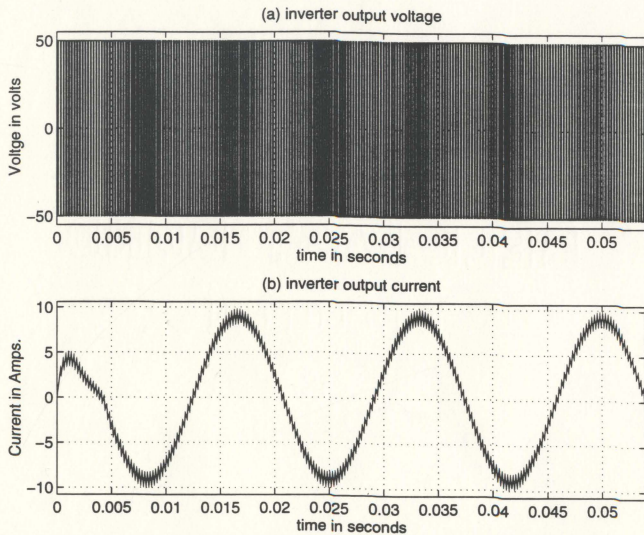


Figure 4.7: Inverter output voltage and current waveforms of the UIS at zero-leading power factor

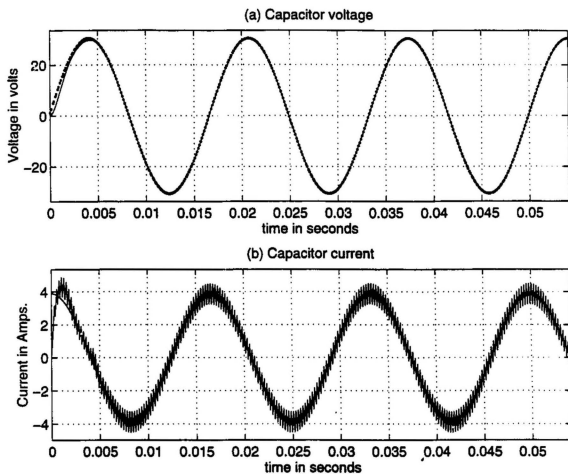


Figure 4.8: Capacitor voltage and current waveforms of the UIS at zero-leading power factor

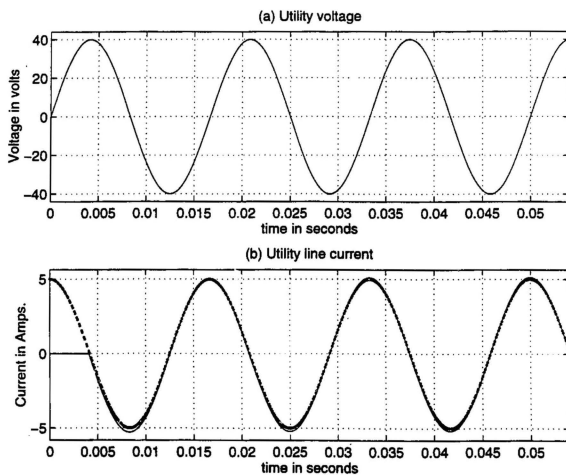


Figure 4.9: Utility voltage and line current waveforms of the UIS at zero-leading power factor

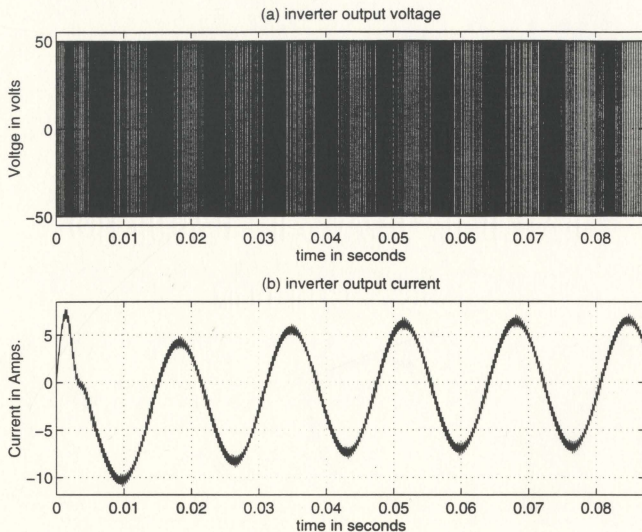


Figure 4.10: Inverter output voltage and current waveforms of the UIS at unity power factor

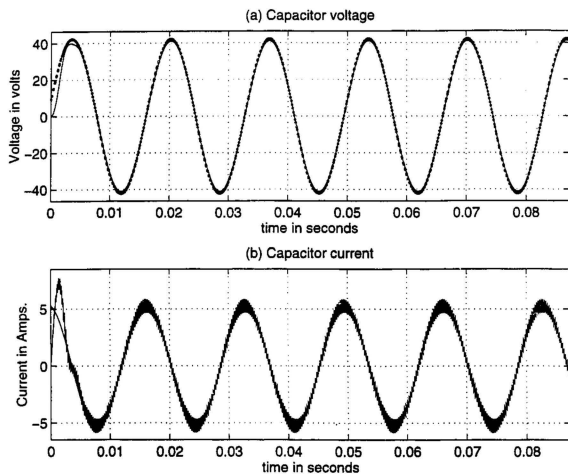


Figure 4.11: Capacitor voltage and current waveforms of the UIS at unity power factor

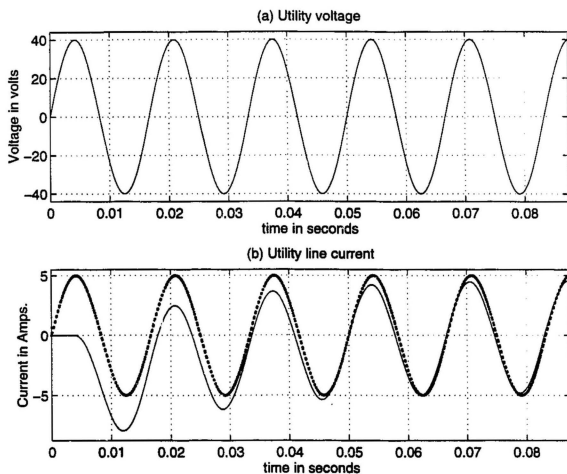


Figure 4.12: Utility voltage and line current waveforms of the UIS at unity power factor

The experimental results were obtained for the following parameters:

$$\begin{array}{lll} L_f = L_2 = 5.0 \text{ mH}, & C_f = 340 \text{ } \mu\text{F}, & V_{dc} = 40 \text{ volts}, \\ V_{ac} = 38 \text{ Volts (Peak)} & F_s = 4.0 \text{ kHz}, & k_{pc} = 2.0, \quad k_{pu} = 5.0. \end{array}$$

Figures 4.13 and 4.14 show the steady-state experimental waveforms of the inverter output voltage and current when the UIS is operating at zero-leading power factor. Currents were measured with a clamp-on meter with a scaling ratio of 1 mV / 1 Ampere. Figure 4.14 shows that the proposed scheme produces a high-quality capacitor voltage with total harmonic distortion less than 2.3 %.

Figure 4.15 shows the utility voltage and current for a 100 % step change in load when the UIS is operating at zero-leading power factor. The indirect control scheme exhibits fast dynamic response and provides steady-state operation within one cycle. The measured THD of the utility line current is 2.1 %. Experimental results of feeding the utility line current at lagging power factor with respect to the utility voltage have been reported in [114].

Figure 4.16 shows the waveforms of the utility line current and voltage for 100 % step change in the line current when the UIS is operating at close to unity power factor. The figure demonstrates that the system is capable of feeding active power into the power grid without deterioration in the quality of the utility current.

4.5 Summary

The control strategy proposed for UPS systems was extended to the single-phase voltage-source UIS to shape and control the utility line current. After establishing the system general model and deriving its low-frequency model, the effects of various filter parameters on the operation of UIS were investigated. It was shown that, for a

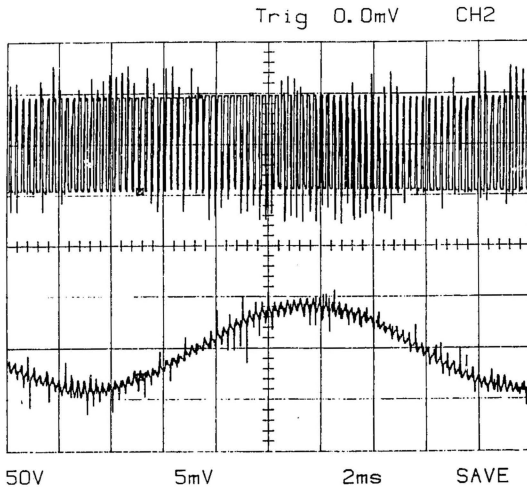


Figure 4.13: Experimental waveforms of the inverter output voltage and current in the single-phase UIS at zero-leading power factor, upper trace: inverter output voltage, lower trace: inverter output current

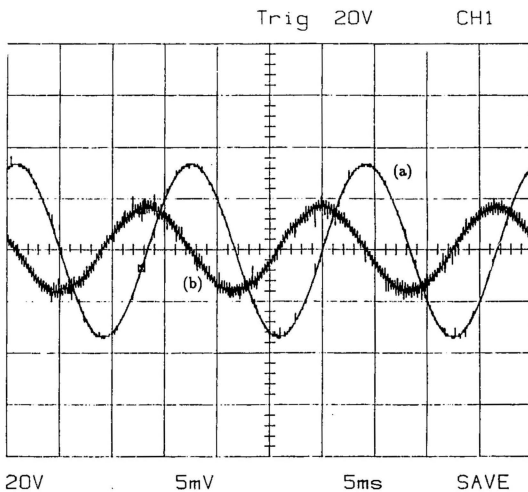


Figure 4.14: Experimental waveforms of the capacitor voltage and current in the single-phase UIS at zero-leading power factor: a) capacitor voltage, b) capacitor current

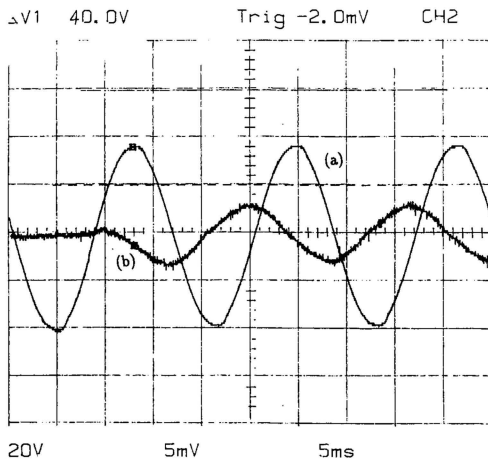


Figure 4.15: Experimental waveforms of the utility voltage and current in the single-phase UIS at zero-leading power factor: a) utility voltage, b) utility line current

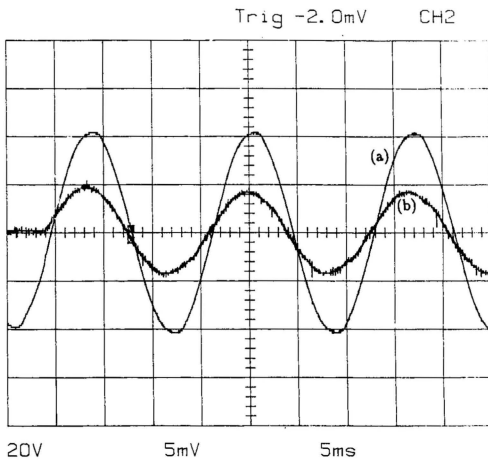


Figure 4.16: Experimental waveforms of the utility voltage and current in the single-phase UIS at unity power factor: a) utility voltage, b) utility line current

wide range of operation of the UIS, the worst-case scenario from the point of view of the filter parameters is when the system is operating at unity power factor.

The incremental dynamics of the power circuit were investigated with the aid of the small-signal model and the root-locus technique. Contrary to what intuition dictates, it was found that employing the utility line current as the feedback variable causes two of the system complex-conjugate poles to move into the right-half of the s -plane, resulting in unstable operation of the UIS.

The proposed control scheme, consisting of the inner capacitor current and outer capacitor voltage feedback loops constituted an indirect control of the utility line current. It was shown that the proposed scheme results in stable and successful operation of the UIS. In addition, it is capable of feeding the utility line current into the AC network at any desired power factor. Furthermore, the scheme ensures good transient and dynamic response and high quality of the utility line current over a wide range of utility network requirements. The proposed scheme lends itself to weak AC network operation because it provides a stiff voltage source across the filter capacitor. Experimental verification of the proposed UIS system demonstrating the capability of the system to feed current at unity and zero-leading power factor into the utility network was presented.

Chapter 5

The Three-Phase Voltage-Source Utility Interactive System

The indirect control scheme proposed in Chapter Four is extended to the three-phase voltage-source utility interactive system (UIS). This chapter deals with the characteristics of this system. Linearized steady-state and small-signal dynamic models are developed for the UIS using the procedures outlined in the previous chapters. Employing the pole-zero map and the root-locus analysis, the characteristics of the three-phase UIS are examined from the point of view of stability of the system.

Simulation results demonstrating the viability of the proposed control scheme for utility interactive applications are presented for unity power factor operation.

5.1 General Model of the Three-Phase UIS

Figure 5.1 shows the power circuit of the three-phase voltage-source UIS. The renewable energy source is interfaced to the utility network through the three-phase voltage-source bridge inverter with output filter $L_f - C_f$.

The renewable energy source is interfaced to the utility network through the three-phase voltage-source bridge inverter with the three-phase output filter ($L_f - C_f$). The

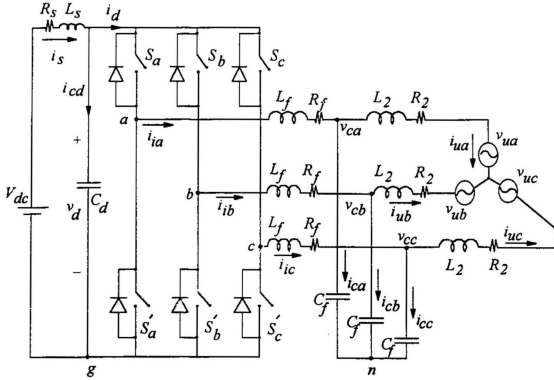


Figure 5.1: Circuit diagram of the three-phase voltage-source utility interactive system

following assumptions are made in deriving the system analytical model:

1. The renewable energy source is modeled as a voltage source.
2. Switching devices are ideal and the effect of snubber circuit is neglected.
3. The ON resistance of the inverter switching devices is included in the resistance associated with the filter inductor.
4. The utility voltage is balanced.

The relationship between the capacitor voltage, source current, and inverter input current on the DC side of the UIS shown in Fig. 5.1 can be written as

$$C_d \frac{dv_d}{dt} = i_s - i_d. \quad (5.1)$$

The inverter input current, i_d , may be expressed in terms of the inverter switching functions and the inverter output current in the three-phases as

$$i_d = S_a^* i_{ia} + S_b^* i_{ib} + S_c^* i_{ic}. \quad (5.2)$$

Substituting Eq. (5.2) into Eq. (5.1) yields

$$C_d \frac{dv_d}{dt} = i_s - (S_a^* i_{ia} + S_b^* i_{ib} + S_c^* i_{ic}). \quad (5.3)$$

The relationship between the source voltage, current, and the capacitor voltage is given by

$$L_s \frac{di_s}{dt} = v_{dc} - (R_s i_s + v_d). \quad (5.4)$$

The governing differential equations of *phase a* on the AC side of the inverter can be written as:

$$L_f \frac{di_{ia}}{dt} + R_f i_{ia} = v_d (S_a^* - \frac{1}{3} (S_a^* + S_b^* + S_c^*)) - v_{cam}, \quad (5.5)$$

$$L_2 \frac{di_{ua}}{dt} + R_2 i_{ua} + v_{uan} = v_{cam}, \quad (5.6)$$

$$C_f \frac{dv_{cam}}{dt} = i_{ia} - i_{ua}. \quad (5.7)$$

Likewise, the governing differential equations for *phase b* and *phase c* can be derived. The system equations of the UIS can be written in state-space representation

as

$$\begin{bmatrix} \dot{i}_{ia} \\ \dot{i}_{ua} \\ \dot{v}_{can} \\ \dot{i}_{ib} \\ \dot{i}_{ub} \\ \dot{v}_{cbn} \\ \dot{i}_{ic} \\ \dot{i}_{uc} \\ \dot{v}_{ccn} \\ \dot{i}_s \\ \dot{v}_d \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{R_s}{L_s} & \frac{1}{L_s} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{R_s}{L_s} & \frac{1}{L_s} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{R_s}{L_s} & \frac{1}{L_s} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{R_s}{L_s} & \frac{1}{C_d} \\ -\frac{S_a^*}{C_d} & 0 & 0 & -\frac{S_a^*}{C_d} & 0 & 0 & -\frac{S_a^*}{C_d} & 0 & 0 & 0 & \frac{1}{C_d} \end{bmatrix}$$

$$\begin{bmatrix} \frac{S_a^* - \frac{1}{s}(S_a^* + S_b^* + S_c^*)}{L_f} \\ 0 \\ 0 \\ \frac{S_b^* - \frac{1}{s}(S_a^* + S_b^* + S_c^*)}{L_f} \\ 0 \\ 0 \\ \frac{S_c^* - \frac{1}{s}(S_a^* + S_b^* + S_c^*)}{L_f} \\ 0 \\ 0 \\ 0 \\ -\frac{1}{L_s} \\ 0 \end{bmatrix} + \begin{bmatrix} \dot{i}_{ia} \\ \dot{i}_{ua} \\ v_{can} \\ \dot{i}_{ib} \\ \dot{i}_{ub} \\ v_{cbn} \\ \dot{i}_{ic} \\ \dot{i}_{uc} \\ v_{ccn} \\ \dot{i}_s \\ v_d \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{L_s} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_s} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L_s} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L_s} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} 0 \\ v_{uan} \\ 0 \\ 0 \\ v_{ubn} \\ 0 \\ 0 \\ v_{ucn} \\ 0 \\ v_{dc} \\ 0 \end{bmatrix}, \quad (5.8)$$

or

$$\dot{\mathbf{x}} = \mathbf{A}^* \mathbf{x} + \mathbf{B} \mathbf{e}. \quad (5.9)$$

For simplicity, the product $\mathbf{B} \mathbf{e}$ is evaluated and denoted by the vector \mathbf{u} , where \mathbf{u} is given by

$$\mathbf{u} = \left[0 \quad \frac{-v_{uan}}{L_s} \quad 0 \quad 0 \quad \frac{-v_{ubn}}{L_s} \quad 0 \quad 0 \quad \frac{-v_{ucn}}{L_s} \quad 0 \quad \frac{v_{dc}}{L_s} \quad 0 \right]^T. \quad (5.10)$$

5.2 Low-Frequency Averaged Model

For the three-phase utility voltage of the form

$$V_{uan} = V_u \cos \omega t, \quad (5.11)$$

$$V_{ubn} = V_u \cos \left(\omega t - \frac{2\pi}{3} \right), \quad (5.12)$$

$$V_{ucn} = V_u \cos \left(\omega t + \frac{2\pi}{3} \right), \quad (5.13)$$

the modulating signal of the respective phases may be expressed as [115]

$$m(t)|_{a,b,c} = V_m \cos \left[\omega t + \gamma + (k-1)\frac{2\pi}{3} \right], \quad (5.14)$$

where

$$k = \begin{cases} 1 & \text{for phase } a, \\ 2 & \text{for phase } b, \\ 3 & \text{for phase } c, \end{cases} \quad (5.15)$$

and γ is the phase angle of the modulating signal with respect to the utility voltage.

The duty cycles for the three phases are given by

$$d_{a,b,c} = \frac{m \cos \left(\omega t + \gamma + (k-1)\frac{2\pi}{3} \right) + 1}{2}, \quad (5.16)$$

where

$$m = \frac{V_m}{V_t}, \quad (5.17)$$

and V_t and V_m are the amplitude of the carrier and modulating signals respectively.

Substituting Eqs. (5.11) to (5.13) and (5.16) into (5.8) gives

$$\begin{bmatrix} \dot{z}_{ia} \\ \dot{z}_{ua} \\ \dot{v}_{can} \\ \dot{z}_{ib} \\ \dot{z}_{ub} \\ \dot{v}_{cbn} \\ \dot{z}_{ic} \\ \dot{z}_{uc} \\ \dot{v}_{ccn} \\ \dot{z}_s \\ \dot{v}_d \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & 0 & 0 \\ 0 & -\frac{R_2}{L_2} & \frac{1}{L_2} & 0 & 0 & 0 \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & 0 & 0 & 0 & -\frac{R_2}{L_2} & \frac{1}{L_2} \\ 0 & 0 & 0 & \frac{1}{C_f} & -\frac{1}{C_f} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{m \cos(\omega t - \gamma) + 1}{2C_d} & 0 & 0 & -\frac{m \cos(\omega t - \gamma - \frac{2\pi}{3}) + 1}{2C_d} & 0 & 0 \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ -\frac{R_f}{L_f} \\ -\frac{R_2}{L_2} \\ \frac{1}{C_f} \\ 0 \\ -\frac{m \cos(\omega t - \gamma + \frac{2\pi}{3}) + 1}{2C_d} \end{bmatrix} + \begin{bmatrix} \dot{z}_{ia} \\ \dot{z}_{ua} \\ \dot{v}_{can} \\ \dot{z}_{ib} \\ \dot{z}_{ub} \\ \dot{v}_{cbn} \\ \dot{z}_{ic} \\ \dot{z}_{uc} \\ \dot{v}_{ccn} \\ \dot{z}_s \\ \dot{v}_d \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{V_u \cos(\omega t)}{L_2} \\ 0 \\ 0 \\ -\frac{V_u \cos(\omega t - \frac{2\pi}{3})}{L_2} \\ 0 \\ 0 \\ -\frac{V_u \cos(\omega t + \frac{2\pi}{3})}{L_2} \\ 0 \\ \frac{v_{dc}}{L_s} \\ 0 \end{bmatrix}, \quad (5.18)$$

or

$$\dot{\mathbf{x}} = \mathbf{A} \mathbf{x} + \mathbf{u}. \quad (5.19)$$

5.3 Low-Frequency Model in the Rotating Frame of Reference

The time-dependent state variables in the stationary frame of reference are transformed to the rotating frame where time-varying quantities at the frequency of the

utility voltage appear as DC quantities. Since the flow of the active and reactive power components of the utility network is of prime interest, the θ - q - d transformation is employed in this chapter. The θ - q - d transformation decomposes the components of the system state variables into an in-phase and in-quadrature to the utility voltage. This decouples the control of the active and reactive power flow of the UIS into the power grid.

The relationship between the variables in the stationary frame of reference and the rotating frame of reference is given by

$$\mathbf{u}_r = \mathbf{T} \mathbf{u}, \quad (5.20)$$

$$\mathbf{x}_r = \mathbf{T} \mathbf{x}, \quad (5.21)$$

where the suffix r denotes variables in the rotating frame of reference.

With the utility voltage chosen to be in alignment with q -axis, the transformation matrix \mathbf{T} is given by

$$\mathbf{T} = \frac{2}{3} \begin{bmatrix} \frac{1}{2} & 0 & 0 & \frac{1}{2} & 0 & 0 \\ 0 & \frac{1}{2} & 0 & 0 & \frac{1}{2} & 0 \\ 0 & 0 & \frac{1}{2} & 0 & 0 & \frac{1}{2} \\ \cos(\omega t) & 0 & 0 & \cos(\omega t - \frac{2\pi}{3}) & 0 & 0 \\ 0 & \cos(\omega t) & 0 & 0 & \cos(\omega t - \frac{2\pi}{3}) & 0 \\ 0 & 0 & \cos(\omega t) & 0 & 0 & \cos(\omega t - \frac{2\pi}{3}) \\ \sin(\omega t) & 0 & 0 & \sin(\omega t - \frac{2\pi}{3}) & 0 & 0 \\ 0 & \sin(\omega t) & 0 & 0 & \sin(\omega t - \frac{2\pi}{3}) & 0 \\ 0 & 0 & \sin(\omega t) & 0 & 0 & \sin(\omega t - \frac{2\pi}{3}) \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$\begin{bmatrix}
\frac{1}{2} & 0 & 0 & 0 & 0 \\
0 & \frac{1}{2} & 0 & 0 & 0 \\
0 & 0 & \frac{1}{2} & 0 & 0 \\
\cos(\omega t + \frac{2\pi}{3}) & 0 & 0 & 0 & 0 \\
0 & \cos(\omega t + \frac{2\pi}{3}) & 0 & 0 & 0 \\
0 & 0 & \cos(\omega t + \frac{2\pi}{3}) & 0 & 0 \\
\sin(\omega t + \frac{2\pi}{3}) & 0 & 0 & 0 & 0 \\
0 & \sin(\omega t + \frac{2\pi}{3}) & 0 & 0 & 0 \\
0 & 0 & \sin(\omega t + \frac{2\pi}{3}) & 0 & 0 \\
0 & 0 & 0 & \frac{3}{2} & 0 \\
0 & 0 & 0 & 0 & \frac{3}{2}
\end{bmatrix}. \quad (5.22)$$

The variables in the rotating frame of reference can be transformed back to the stationary frame of reference using the following relationships:

$$\mathbf{x} = \mathbf{T}^{-1} \mathbf{x}_r, \quad (5.23)$$

$$\mathbf{u} = \mathbf{T}^{-1} \mathbf{u}_r, \quad (5.24)$$

where the inverse of the transformation matrix, \mathbf{T}^{-1} , is given by

$$\mathbf{T}^{-1} = \begin{bmatrix}
1 & 0 & 0 & \cos(\omega t) & 0 & 0 & \sin(\omega t) \\
0 & 1 & 0 & 0 & \cos(\omega t) & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & \cos(\omega t) & 0 \\
1 & 0 & 0 & \cos(\omega t - \frac{2\pi}{3}) & 0 & 0 & \sin(\omega t - \frac{2\pi}{3}) \\
0 & 1 & 0 & 0 & \cos(\omega t - \frac{2\pi}{3}) & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & \cos(\omega t - \frac{2\pi}{3}) & 0 \\
1 & 0 & 0 & \cos(\omega t + \frac{2\pi}{3}) & 0 & 0 & \sin(\omega t + \frac{2\pi}{3}) \\
0 & 1 & 0 & 0 & \cos(\omega t + \frac{2\pi}{3}) & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & \cos(\omega t + \frac{2\pi}{3}) & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}$$

$$\begin{bmatrix}
 0 & 0 & 0 & 0 \\
 \sin(\omega t) & 0 & 0 & 0 \\
 0 & \sin(\omega t) & 0 & 0 \\
 0 & 0 & 0 & 0 \\
 \sin(\omega t - \frac{2\pi}{3}) & 0 & 0 & 0 \\
 0 & \sin(\omega t - \frac{2\pi}{3}) & 0 & 0 \\
 0 & 0 & 0 & 0 \\
 \sin(\omega t + \frac{2\pi}{3}) & 0 & 0 & 0 \\
 0 & \sin(\omega t + \frac{2\pi}{3}) & 0 & 0 \\
 0 & 0 & 1 & 0 \\
 0 & 0 & 0 & 1
 \end{bmatrix} \quad (5.25)$$

Substituting Eqs. (5.23) and (5.24) into (5.19) and rearranging, the system state-space equation in the rotating frame of reference is represented by

$$\dot{\mathbf{x}}_r = \mathbf{A}_r \mathbf{x}_r + \mathbf{u}_r. \quad (5.26)$$

For a balanced three-phase system, the zero-sequence component of the variables in the rotating frame are null, hence Eq. (5.26) can be written as

$$\dot{\mathbf{x}}_{rr} = \mathbf{A}_{rr} \mathbf{x}_{rr} + \mathbf{u}_{rr}, \quad (5.27)$$

where the subscript *rr* denotes the reduced system of equations in the rotating frame of reference, and

$$\mathbf{A}_{rr} = \begin{bmatrix}
 -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & -\omega & 0 & 0 & 0 & \frac{m \cos \gamma}{2 L_f} \\
 0 & -\frac{R_f}{L_f} & \frac{1}{L_f} & 0 & -\omega & 0 & 0 & 0 \\
 \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 & -\omega & 0 & 0 \\
 \omega & 0 & 0 & -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & -\frac{m \sin \gamma}{2 L_f} \\
 0 & \omega & 0 & 0 & -\frac{R_f}{L_f} & \frac{1}{L_f} & 0 & 0 \\
 0 & 0 & \omega & \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & -\frac{R_s}{L_s} & -\frac{1}{L_s} \\
 -\frac{3m \cos \gamma}{4 C_d} & 0 & 0 & \frac{3m \sin \gamma}{4 C_d} & 0 & 0 & \frac{1}{C_d} & 0
 \end{bmatrix}, \quad (5.28)$$

$$\mathbf{u}_{rr} = \begin{bmatrix} 0 & -\frac{V_n}{L_2} & 0 & 0 & 0 & 0 & \frac{V_{dc}}{L_s} & 0 \end{bmatrix}^T, \quad (5.29)$$

$$\mathbf{x}_{rr} = \begin{bmatrix} i_{iq} & i_{uq} & v_{cq} & i_{id} & i_{ud} & v_{cd} & i_s & v_d \end{bmatrix}^T. \quad (5.30)$$

The system equations of the UIS in the rotating frame of reference lead to the equivalent circuit shown in Fig. 5.2. The circuit can be used to investigate the performance of the UIS in the same manner as the vector control technique in AC motor drives. Notice that the system inputs are the DC source voltage, the modulation index, m , the phase angle of the modulating signal, Γ , with respect to the utility voltage, the angular frequency, ω , and the amplitude of the utility voltage, v_u .

5.4 Linearized Low-Frequency Model

Equation (5.28) is linearized using perturbation and small-signal approximation. The system variables are perturbing around their nominal operating points as follows:

$$i_{iq} = I_{iq} + \tilde{i}_{iq}, \quad (5.31)$$

$$i_{uq} = I_{uq} + \tilde{i}_{uq}, \quad (5.32)$$

$$v_{cq} = V_{cq} + \tilde{v}_{cq}, \quad (5.33)$$

$$i_{id} = I_{id} + \tilde{i}_{id}, \quad (5.34)$$

$$i_{vd} = I_{vd} + \tilde{i}_{vd}, \quad (5.35)$$

$$v_{cd} = V_{cd} + \tilde{v}_{cd}, \quad (5.36)$$

$$i_s = I_s + \tilde{i}_s, \quad (5.37)$$

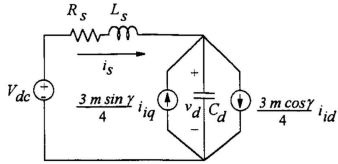
$$v_d = V_d + \tilde{v}_d, \quad (5.38)$$

$$m = M + \tilde{m}, \quad (5.39)$$

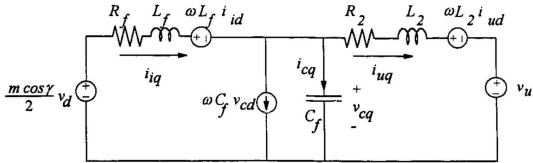
$$\gamma = \Gamma + \tilde{\gamma}, \quad (5.40)$$

$$v_{dc} = V_{dc} + \tilde{v}_{dc}, \quad (5.41)$$

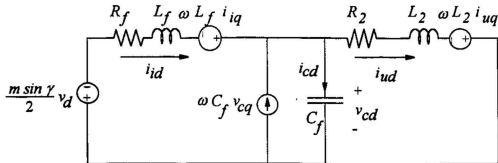
$$v_u = V_u + \tilde{v}_u, \quad (5.42)$$



(a)



(b)



(c)

Figure 5.2: Equivalent circuit model of the three-phase voltage-source UIS in the rotating frame of reference

$$\omega = \Omega + \tilde{\omega}. \quad (5.43)$$

Substituting Eqs. (5.31) to (5.42) into (5.27) results in the following equation

$$\begin{bmatrix} \dot{\tilde{i}}_{iq} \\ \dot{\tilde{i}}_{uq} \\ \dot{\tilde{v}}_{cq} \\ \dot{\tilde{i}}_{id} \\ \dot{\tilde{i}}_{ud} \\ \dot{\tilde{v}}_{cd} \\ \dot{\tilde{i}}_s \\ \dot{\tilde{v}}_d \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & -(\Omega + \tilde{\omega}) \\ 0 & -\frac{R_2}{L_2} & \frac{1}{L_2} & 0 \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 \\ \Omega + \tilde{\omega} & 0 & 0 & -\frac{R_f}{L_f} \\ 0 & \Omega + \tilde{\omega} & 0 & 0 \\ 0 & 0 & \Omega + \tilde{\omega} & \frac{1}{C_f} \\ 0 & 0 & 0 & 0 \\ -\frac{3(M+\tilde{m})\cos(\Gamma+\tilde{\gamma})}{4C_d} & 0 & 0 & \frac{3(M+\tilde{m})\sin(\Gamma+\tilde{\gamma})}{4C_d} \end{bmatrix} \begin{bmatrix} 0 & 0 & 0 & \frac{(M+\tilde{m})\cos(\Gamma+\tilde{\gamma})}{2L_f} \\ -(\Omega + \tilde{\omega}) & 0 & 0 & 0 \\ 0 & -(\Omega + \tilde{\omega}) & 0 & 0 \\ 0 & -\frac{1}{L_f} & 0 & -\frac{(M+\tilde{m})\sin(\Gamma+\tilde{\gamma})}{2L_f} \\ -\frac{R_2}{L_2} & \frac{1}{L_2} & 0 & 0 \\ -\frac{1}{C_f} & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_s}{L_s} & -\frac{1}{L_s} \\ 0 & 0 & \frac{1}{C_d} & 0 \end{bmatrix} + \begin{bmatrix} I_{iq} + \tilde{i}_{iq} \\ I_{uq} + \tilde{i}_{uq} \\ V_{cq} + \tilde{v}_{cq} \\ I_{id} + \tilde{i}_{id} \\ I_{ud} + \tilde{i}_{ud} \\ V_{cd} + \tilde{v}_{cd} \\ I_s + \tilde{i}_s \\ V_d + \tilde{v}_d \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{V_u + \tilde{v}_u}{L_2} \\ 0 \\ 0 \\ 0 \\ \frac{V_{dc} + \tilde{v}_{dc}}{L_s} \\ 0 \end{bmatrix}. \quad (5.44)$$

First-order approximation can be applied to each element of Eq. (5.44) to obtain a linearized system model. For example, the element (1,8) of the \mathbf{A}_{rr} matrix of Eq. (5.44) can be written as

$$(M + \tilde{m}) \cos(\Gamma + \tilde{\gamma}) = (M + \tilde{m})(\cos \Gamma \cos \tilde{\gamma} - \sin \Gamma \sin \tilde{\gamma}). \quad (5.45)$$

For sufficiently small $\tilde{\gamma}$, $\cos \tilde{\gamma} \cong 1$ and $\sin \tilde{\gamma} \cong \tilde{\gamma}$. Neglecting non-linear terms, Eq. 5.45 can be approximated as

$$(M + \tilde{m}) \cos(\Gamma + \tilde{\gamma}) = M \cos \Gamma - M \sin \Gamma \sin \tilde{\gamma} + \cos \Gamma \tilde{\gamma}. \quad (5.46)$$

An approximate linearized model of the three-phase voltage-source utility interactive system in the rotating frame of reference is represented in the general form as

$$\begin{aligned} \dot{\tilde{\mathbf{x}}}_{rr} = & \mathbf{A}_{ss} \mathbf{X}_{rr} + \mathbf{U}_{rr} + \mathbf{A}_{ss} \tilde{\mathbf{x}}_{rr} + \mathbf{A}_m \mathbf{X}_{rr} \tilde{m} + \mathbf{A}_\gamma \mathbf{X}_{rr} \tilde{\gamma} + \mathbf{A}_\omega \mathbf{X}_{rr} \dot{\omega} \\ & + \mathbf{A}_{vu} \tilde{v}_u + \mathbf{A}_{vdc} \tilde{v}_{dc}, \end{aligned} \quad (5.47)$$

where

$$\mathbf{A}_{ss} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & -\Omega & 0 & 0 & 0 & \frac{M \cos \Gamma}{2 L_f} \\ 0 & -\frac{R_2}{L_2} & \frac{1}{L_2} & 0 & -\Omega & 0 & 0 & 0 \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 & -\Omega & 0 & 0 \\ \Omega & 0 & 0 & -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 & -\frac{M \sin \Gamma}{2 L_f} \\ 0 & 0 & \Omega & 0 & -\frac{R_2}{L_2} & \frac{1}{L_2} & 0 & 0 \\ 0 & 0 & \Omega & \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{R_s}{L_s} & -\frac{1}{L_s} \\ -\frac{3M \cos \Gamma}{4 C_d} & 0 & 0 & \frac{3M \sin \Gamma}{4 C_d} & 0 & 0 & \frac{1}{C_d} & 0 \end{bmatrix}, \quad (5.48)$$

$$\mathbf{X}_{rr} = [I_{iq} \ I_{uq} \ V_{cq} \ I_{id} \ I_{ud} \ V_{cd} \ I_s \ V_d]^T, \quad (5.49)$$

$$\mathbf{U}_{rr} = \left[0 \ -\frac{V_n}{L_2} \ 0 \ 0 \ 0 \ 0 \ \frac{V_{dc}}{L_s} \ 0 \right]^T, \quad (5.50)$$

$$\mathbf{A}_m = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & \frac{\cos \Gamma}{2 L_f} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{\sin \Gamma}{2 L_f} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{3 \cos \Gamma}{4 C_d} & 0 & 0 & \frac{3 \sin \Gamma}{4 C_d} & 0 & 0 & 0 \end{bmatrix}, \quad (5.51)$$

$$\mathbf{A}_\gamma = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{M \sin \Gamma}{2L_f} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{M \cos \Gamma}{2L_f} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{3M \sin \Gamma}{4C_d} & 0 & 0 & \frac{3M \cos \Gamma}{4C_d} & 0 & 0 & 0 & 0 \end{bmatrix}, \quad (5.52)$$

$$\mathbf{A}_\omega = \begin{bmatrix} 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad (5.53)$$

$$\mathbf{A}_{vu} = \begin{bmatrix} 0 & -\frac{1}{L_2} & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T, \quad (5.54)$$

and

$$\mathbf{A}_{vdc} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_2} & 0 \end{bmatrix}^T. \quad (5.55)$$

5.3 Steady-State Model and Analysis

The steady-state variables are obtained from Eq. (5.47) by setting all perturbations to zero. The resulting steady-state model in the rotating frame of reference is represented by

$$\mathbf{A}_{ss} \mathbf{X}_{rr} + \mathbf{U}_{rr} = 0. \quad (5.56)$$

Assuming that the resistances associated with the filter inductors on both the AC and DC side of the inverter have negligible effect on the steady-state variables in the rotating frame of reference, the steady-state variables in the d - q axes are obtained

from Eq. (5.56) as

$$I_{iq} \cong \frac{(X_{lf2} - X_{cf}) M V_{dc} \sin \Gamma}{2 (X_{cf} (X_{lf1} + X_{lf2}) - X_{lf1} X_{lf2})}, \quad (5.57)$$

$$I_{id} \cong \frac{1}{2} \frac{(X_{cf} - X_{lf2}) M V_{dc} \cos \Gamma - 2 V_u X_{cf}}{X_{cf} (X_{lf1} + X_{lf2}) - X_{lf1} X_{lf2}}, \quad (5.58)$$

$$I_{uq} \cong \frac{M V_{dc} X_{cf} \sin \Gamma}{2 (X_{cf} (X_{lf1} + X_{lf2}) - X_{lf1} X_{lf2})}, \quad (5.59)$$

$$I_{ud} \cong \frac{2 V_u (X_{lf1} - X_{cf}) + M V_{dc} \cos \Gamma}{2 (X_{cf} (X_{lf1} + X_{lf2}) - X_{lf1} X_{lf2})}, \quad (5.60)$$

$$V_{cq} \cong \frac{X_{cf} (2 V_u X_{lf1} + M V_{dc} \cos \Gamma X_{lf2})}{2 (X_{cf} (X_{lf1} + X_{lf2}) - X_{lf1} X_{lf2})}, \quad (5.61)$$

$$V_{cd} \cong \frac{X_{cf} M V_{dc} X_{lf2} \sin \Gamma}{2 (X_{lf1} X_{lf2} - X_{cf} (X_{lf1} + X_{lf2}))}, \quad (5.62)$$

$$I_s \cong \frac{3}{4} \frac{X_{cf} M V_{dc} X_{lf2} \sin \Gamma}{X_{lf1} (2 X_{cf} - X_{lf1})}, \quad (5.63)$$

$$V_d \cong V_{dc}. \quad (5.64)$$

Equations (5.57) to (5.63) are useful in determining the system steady-state quantities and establishing the quiescent operating point of the system. Equations (5.59) and (5.60) represent the q - and d - components of the current injected into the power grid respectively. For a unity power factor operation, I_{ud} , is set to zero. Given the magnitude of the current injected into the power grid and the system parameters, Eqs. (5.59) and (5.60) can be solved to determine M and Γ . Similarly, for zero-leading power factor operation, I_{uq} , is set to zero.

Equation (5.63) shows that for zero-leading power factor operation (i.e., $\Gamma = 0$), the current drawn from the DC source is zero. In practice, a small current will be drawn from the DC source to supply the switching losses and power lost in the resistances associated with the filter inductors and the isolation transformer.

5.6 Small-Signal Model and Analysis

The small-signal dynamic model of the UIS system is obtained from Eq. (5.47) as

$$\dot{\tilde{\mathbf{x}}_{rr}} = \mathbf{A}_{ss} \tilde{\mathbf{x}}_{rr} + \mathbf{A}_m \mathbf{X}_{rr} \tilde{m} + \mathbf{A}_\gamma \mathbf{X}_{rr} \tilde{\gamma} + \mathbf{A}_\omega \mathbf{X}_{rr} \tilde{\omega} + \mathbf{A}_{vu} \tilde{v}_u + \mathbf{A}_{vdc} \tilde{v}_{dc}. \quad (5.65)$$

Equation (5.65) can be used to derive the transfer functions that relate the incremental changes in the control signal or any of the disturbances to the incremental variation of the state variables.

For example, the transfer function of the incremental variation in the magnitude of the control signal to the incremental changes in the state variables is obtained by setting all other disturbances to zero (i.e., $\tilde{\gamma} = \tilde{\omega} = \tilde{v}_u = \tilde{v}_{dc} = 0$). The resultant small-signal model is given by

$$\dot{\tilde{\mathbf{x}}_{rr}} = \mathbf{A}_{ss} \tilde{\mathbf{x}}_{rr} + \mathbf{A}_m \mathbf{X}_{rr} \tilde{m}, \quad (5.66)$$

which upon substituting \mathbf{A}_{ss} , \mathbf{A}_m , and \mathbf{X}_{rr} from Eqs. (5.48), (5.51), and (5.56) respectively into Eq. (5.66) gives

$$\begin{bmatrix} \dot{\tilde{i}}_{iq} \\ \dot{\tilde{i}}_{uq} \\ \dot{\tilde{v}}_{cq} \\ \dot{\tilde{i}}_{id'} \\ \dot{\tilde{i}}_{ud} \\ \dot{\tilde{v}}_{cd} \\ \dot{\tilde{i}}_s \\ \dot{\tilde{v}}_d \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & -\Omega & 0 & 0 & 0 & \frac{M \cos \Gamma}{2 L_f} \\ 0 & -\frac{R_2}{L_2} & \frac{1}{L_2} & 0 & -\Omega & 0 & 0 & 0 \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 & -\Omega & 0 & 0 \\ \Omega & 0 & 0 & -\frac{R_f}{L_f} & 0 & -\frac{R_2}{L_2} & 0 & -\frac{M \sin \Gamma}{2 L_f} \\ 0 & \Omega & 0 & 0 & -\frac{R_2}{L_2} & \frac{1}{L_2} & 0 & 0 \\ 0 & 0 & \Omega & \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{R_s}{L_s} & -\frac{1}{L_s} \\ -\frac{3}{4} \frac{M \cos \Gamma}{4 C_d} & 0 & 0 & \frac{3}{4} \frac{M \sin \Gamma}{4 C_d} & 0 & 0 & \frac{1}{C_d} & 0 \end{bmatrix}$$

$$\begin{bmatrix} \tilde{i}_{iq} \\ \tilde{i}_{uq} \\ \tilde{v}_{cq} \\ \tilde{i}_{id} \\ \tilde{i}_{ud} \\ \tilde{v}_{cd} \\ \tilde{i}_s \\ \tilde{v}_d \end{bmatrix} + \begin{bmatrix} \frac{V_d \cos \Gamma}{2 L_f} \\ 0 \\ 0 \\ -\frac{V_d \sin \Gamma}{2 L_f} \\ 0 \\ 0 \\ 0 \\ \frac{3}{4 C_d} (\sin \Gamma I_{id} - \cos \Gamma I_{iq}) \end{bmatrix}. \quad (5.67)$$

Taking the Laplace transform of Eq. (5.66) and rearranging, the transfer function of the incremental variation in the modulation index to incremental changes in the state variables is given by

$$\frac{\tilde{\mathbf{x}}_{rr}(s)}{\tilde{m}(s)} = (s \mathbf{I} - \mathbf{A}_{ss})^{-1} \mathbf{A}_m \mathbf{X}_{rr}. \quad (5.68)$$

Equation (5.67) shows that the transfer function of the incremental dynamics of the state variables of the system is dependent on the steady-state values of the inverter output current (I_{iq} and I_{id}), the voltage across the input DC capacitor (V_d), and the phase angle of the modulating signal (Γ) with respect to the utility voltage. Given these values, the transfer function can be derived from Eq. (5.68) to investigate the incremental dynamics of the state variables. In particular, the magnitude of the utility line current, capacitor voltage, and capacitor current are examined.

The magnitude of the variable y related to its d - and q -components in the rotating frame of reference is given by

$$y = \sqrt{y_d^2 + y_q^2}. \quad (5.69)$$

Perturbing the variable y around its nominal operating point as

$$y = Y + \tilde{y}, \quad (5.70)$$

$$y_d = Y_d + \tilde{y}_d, \quad (5.71)$$

$$y_q = Y_q + \tilde{y}_q, \quad (5.72)$$

and substituting into Eq. (5.69), the first-order approximation of the resultant equation is given by

$$\tilde{y} \cong \frac{1}{\sqrt{Y_d^2 + Y_q^2}} (Y_d \tilde{y}_d + Y_q \tilde{y}_q). \quad (5.73)$$

The transfer function of the incremental changes in the magnitude of y due to incremental changes in the control signal is given by

$$\frac{\tilde{y}(s)}{\tilde{m}(s)} \cong \frac{1}{\sqrt{Y_d^2 + Y_q^2}} (Y_d \frac{\tilde{y}_d(s)}{\tilde{m}(s)} + Y_q \frac{\tilde{y}_q(s)}{\tilde{m}(s)}). \quad (5.74)$$

Equation (5.74) shows that the transfer function of the generic variable y is composed of the transfer function of its direct and quadrature components.

The characteristics of the UIS for different modes of operation can be examined with the aid of the pole-zero map representation and the root-locus plots of the transfer function under investigation. In the following sections, the incremental dynamics of the power circuit state variables are examined for the following system parameters:

$$\begin{array}{llll} L_s=10.0 \text{ mH}, & C_d=5000 \mu\text{F}, & L_f=L_2=5.0 \text{ mH}, & C_f=300.0 \mu\text{F}, \\ V_{dc}=200 \text{ Volts}, & V_u=110 \text{ Volts (RMS)}, & I_u=7.07 \text{ Amps (RMS)}. \end{array}$$

5.6.1 Incremental Dynamics of the Utility Line Current

The transfer function of the incremental changes in the magnitude of the utility line current due to incremental changes in the modulation index is obtained using Eq. (5.74) where the generic variable, y , is replaced by the utility line current, i_u , and is given as

$$\frac{\tilde{i}_u(s)}{\tilde{m}(s)} \cong \frac{1}{\sqrt{I_{ud}^2 + I_{uq}^2}} (I_{ud} \frac{\tilde{i}_{ud}(s)}{\tilde{m}(s)} + I_{uq} \frac{\tilde{i}_{uq}(s)}{\tilde{m}(s)}). \quad (5.75)$$

The terms $\frac{\tilde{i}_{ud}(s)}{\tilde{m}(s)}$ and $\frac{\tilde{i}_{uq}(s)}{\tilde{m}(s)}$ are obtained from the second and fifth rows of Eq. (5.68).

Equation (5.75) can be represented in the general form

$$G_{iu}(s) = \frac{\hat{i}_u(s)}{\hat{m}(s)} = \frac{k_{iu} G_{iu(num)}(s)}{G_{iu(den)}(s)}, \quad (5.76)$$

where k_{iu} is a constant, $G_{iu(num)}(s)$, and $G_{iu(den)}(s)$ can be written as

$$G_{iu(num)}(s) = (s + \alpha_{z1u})((s + \alpha_{z2u})^2 + \omega_{z2u}^2)((s + \alpha_{z3u})^2 + \omega_{z3u}^2), \quad (5.77)$$

$$G_{iu(den)}(s) = ((s + \alpha_{p1})^2 + \omega_{p1}^2)((s + \alpha_{p2})^2 + \omega_{p2}^2)((s + \alpha_{p3})^2 + \omega_{p3}^2)((s + \alpha_{p4})^2 + \omega_{p4}^2). \quad (5.78)$$

Figure 5.3 shows the pole-zero map of the transfer function of the incremental changes in the utility line current due to incremental changes in the modulation index for unity power factor operation. The figure shows that the transfer function has four complex pole-pairs, three complex conjugate zero-pairs and a negative real zero. All of the system poles and zeros are located in the left-hand side of the s-plane. Figure 5.4 shows the pole-zero map of the UIS for zero-leading power factor operation. The figure shows that for this mode of operation, a zero is located in the right-hand side of the s-plane.

Figure 5.5 shows the root locus of the transfer function $G_{iu}(s)$ when the utility line current is used as the feedback variable, and the system is operating at unity power factor. The figure was obtained for a 10% variation in the modulation index. The figure shows that closing the feedback loop around the utility line current causes four of the system poles to move to the right-hand side of the s-plane, resulting in unstable operation of the UIS system. The root locus of the utility current when the system is operated at zero-leading power factor is shown in Fig. 5.6. The figure shows that the positive real zero causes one of the system poles to move to the right-hand side of the s-plane resulting in unstable operation as well.

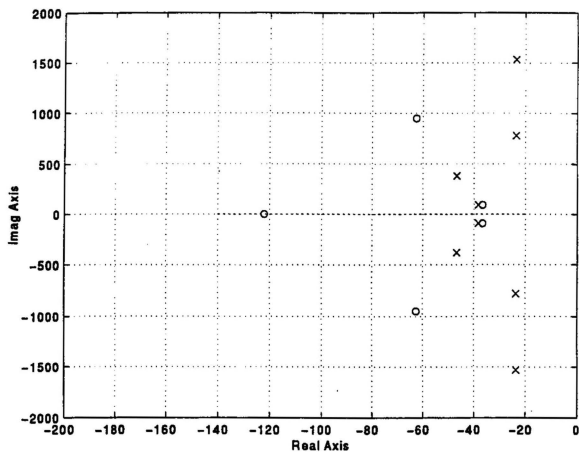


Figure 5.3: Pole-zero map of the transfer function of the incremental variation in the utility current for unity power factor operation

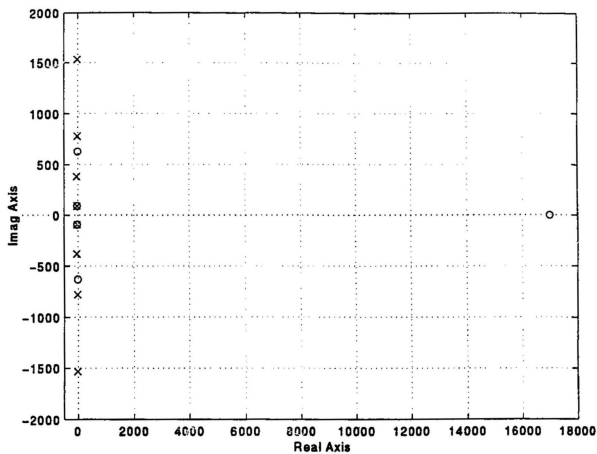


Figure 5.4: Pole-zero map of the transfer function of the incremental variation in the utility current for zero-leading power factor operation

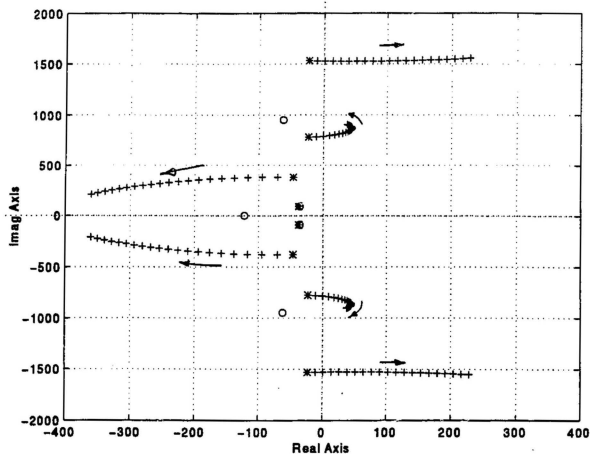


Figure 5.5: Root locus of the incremental variation in the utility line current for incremental changes in the control signal: unity power factor operation

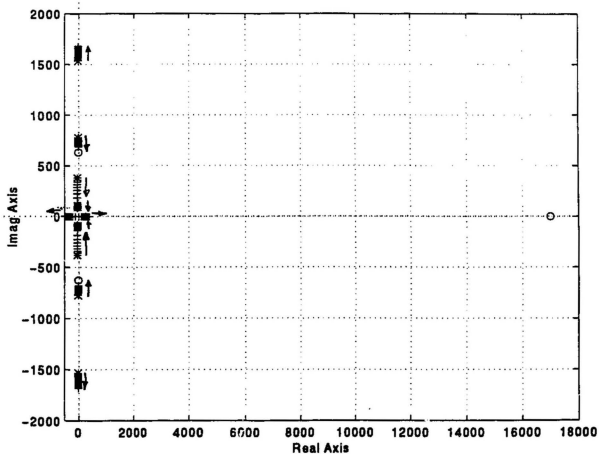


Figure 5.6: Root locus of the incremental variation in the utility line current for incremental changes in the control signal: zero-leading power factor operation

Figure 5.7 shows the time-domain simulation of the utility current when it is used as the feedback variable. The figure shows that for both unity and zero-leading power factor operation, the utility line current rises in an exponentially sinusoidal fashion confirming the instability of the system.

5.6.2 Incremental Dynamics of the Capacitor Voltage

The transfer function of the magnitude of the capacitor voltage due to incremental changes in the modulation index is obtained from the third and sixth rows of Eq. (5.68). Using Eq. (5.74), the transfer function is expressed as

$$\frac{\tilde{v}_c(s)}{\tilde{m}(s)} = G_{vc}(s) = \frac{1}{\sqrt{V_{cd}^2 + V_{cq}^2}} (V_{cd} \frac{\tilde{v}_{cd}(s)}{\tilde{m}(s)} + V_{cq} \frac{\tilde{v}_{cq}(s)}{\tilde{m}(s)}), \quad (5.79)$$

or

$$G_{vc}(s) = \frac{k_{vc} G_{vc(num)}(s)}{G_{vc(den)}(s)}, \quad (5.80)$$

where k_{vc} is a constant, $G_{vc(den)}(s)$ is the same as $G_{iu(den)}(s)$ (Eq. (5.78)), and $G_{vc(num)}(s)$ can be expressed as

$$G_{vc(num)}(s) = ((s + \alpha_{z1v})^2 + \omega_{z1v}^2)((s + \alpha_{z2v})^2 + \omega_{z2v}^2)((s + \alpha_{z3v})^2 + \omega_{z3v}^2). \quad (5.81)$$

The pole-zero map of Eq. (5.79) for unity power factor operation is shown in Fig. 5.8. The figure shows that the transfer function has three complex conjugate zeros. The pole-zero map for zero-leading power factor is shown in Fig. 5.9. Figures 5.8 and 5.9 show that the mode of operation has negligible effect on the location of the system poles. However, for zero-leading power factor operation, two of the complex conjugate zeros are located closer to the imaginary axis of the s-plane, hence resulting in faster dynamic response.

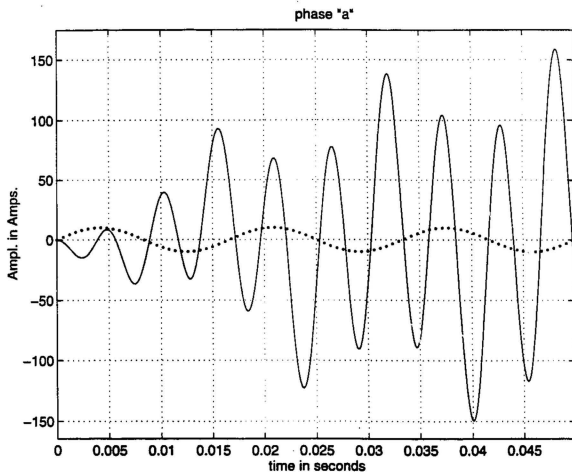


Figure 5.7: Time-domain simulation of the utility line current with the utility line current i_a as the feedback variable: unity power factor operation

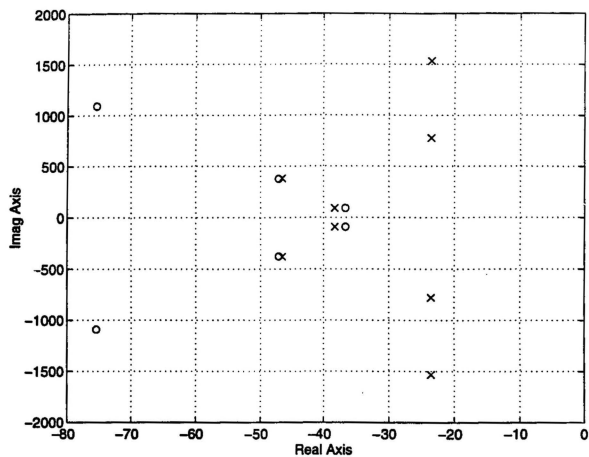


Figure 5.8: Pole-zero map of the transfer function of the capacitor voltage for unity power factor operation

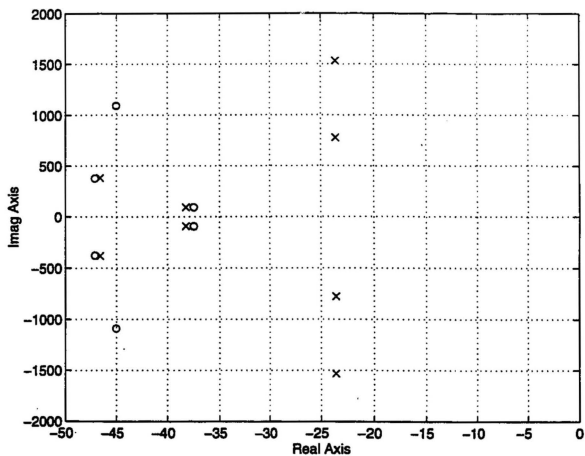


Figure 5.9: Pole-zero map of the transfer function of the capacitor voltage for zero-leading power factor operation

The root locus of the capacitor voltage for unity power factor operation and 10 % variation in the modulation index is shown in Fig. 5.10. The figure shows that employing the capacitor voltage as the only feedback variable in the control circuit causes two of the system complex pole-pairs to move to the right-hand side of the s-plane resulting in unstable operation. Figure 5.11 shows the root locus of the capacitor voltage for zero-leading power factor operation. The figure shows that two of the system complex conjugate poles move along the imaginary axis of the s-plane, resulting in an oscillatory behaviour of the capacitor voltage.

Figure 5.12 shows the time-domain simulation of the UIS operating at zero-leading power factor with the capacitor voltage employed as the only feedback variable. The figure reveals the oscillatory behaviour of the capacitor voltage which is unacceptable for UIS applications.

5.6.3 Incremental Dynamics of the Capacitor Current

The transfer function of the incremental changes in the magnitude of the capacitor current is obtained from the transfer function of the capacitor voltage as

$$G_{ic}(s) = C_f s G_{vc}(s). \quad (5.82)$$

The pole-zero map of Eq. (5.82) is the same as that obtained for the capacitor voltage (Figs. 5.8, 5.9) with the addition of a zero at the origin.

The root loci of the incremental changes in the magnitude of the capacitor current due to incremental changes in the modulation index for unity and zero-leading power factor operation are shown in Figs. 5.13 and 5.14 respectively. The figures show that employing the capacitor current as the only feedback variable results in moving the system poles further into the left-hand side of the s-plane, resulting in stable

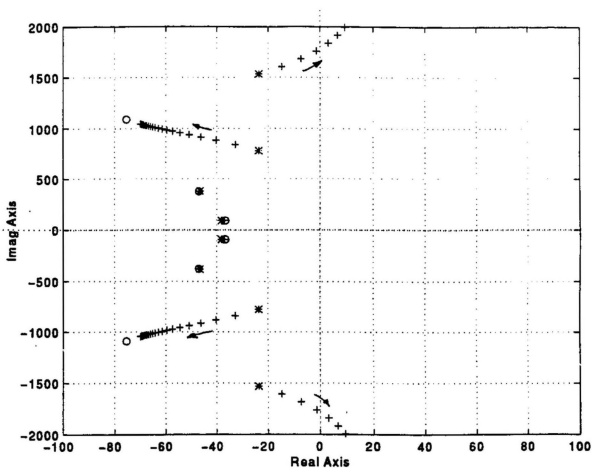


Figure 5.10: Root locus of the incremental variation in the capacitor voltage for incremental change in the in the control signal: unity power factor operation

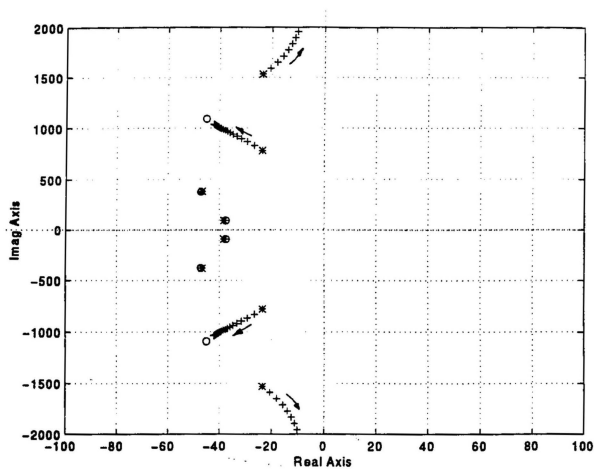


Figure 5.11: Root locus of the incremental variation in the capacitor voltage for incremental change in the control signal: zero leading power factor operation

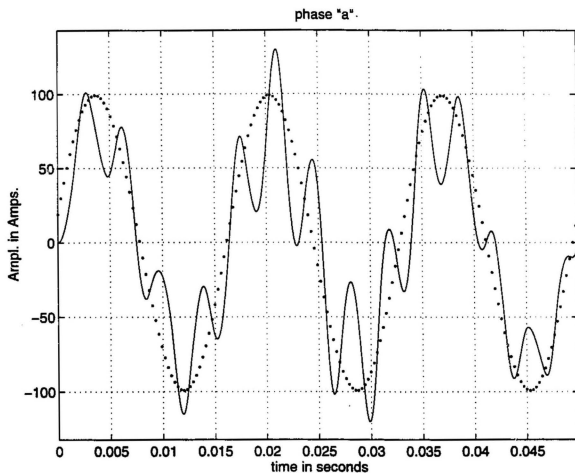


Figure 5.12: Time domain simulation of the capacitor voltage with the capacitor voltage as the only feedback variable: zero-leading power factor operation

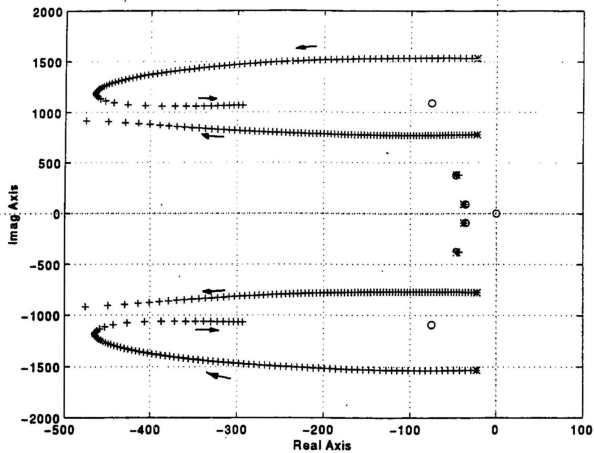


Figure 5.13: Root locus of the incremental variation of the capacitor current due to incremental changes in the control signal: unity power factor operation

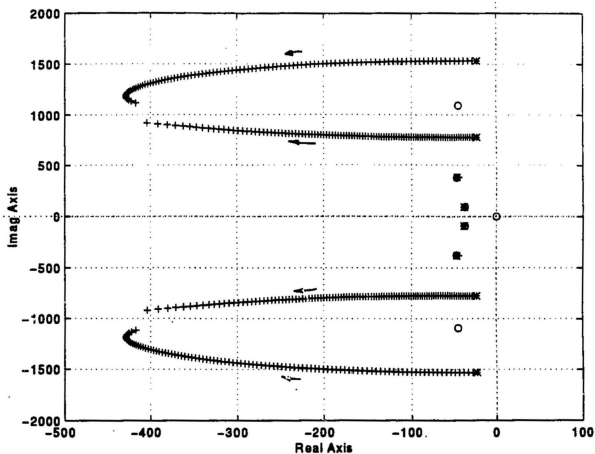


Figure 5.14: Root locus of the incremental variation of the capacitor current due to incremental changes in the control signal: zero-leading power factor operation

operation of the UIS.

In order to ensure that the capacitor voltage faithfully tracks its reference waveform, an outer capacitor voltage feedback loop is incorporated. The outer feedback loop also guarantees a stiff sinusoidal capacitor voltage, and hence a sinusoidal utility line current. Furthermore, it acts as an active damping scheme to prevent resonance between the UIS filter shunt capacitor and other components connected to the utility network. The resulting closed-loop control scheme is shown in Fig. 5.18.

The Bode plots of the open-loop transfer function (the reduced order) of the capacitor current at unity and zero-leading power factor operation are shown in Fig. 5.15. The figure shows that the loop has slightly larger bandwidth when the system is operating at unity power factor.

Figure 5.16 shows the Bode plot of the closed-loop transfer function of the inner current loop. The figure shows that the inner current loop possesses unity gain over a relatively small range of frequencies especially when the system is operating at zero-leading power factor. The bandwidth of the inner current loop can be increased by using a proportional controller, k_{pc} , in the feed-forward path of the loop as shown in Fig. 5.17.

5.7 Computer Simulation

The operation of the three-phase voltage source UIS shown in Fig. 5.18 is simulated to obtain various waveforms in the UIS. Simulation waveforms are provided for the worst-case operating condition of unity power factor. The waveforms were obtained by solving Eq. (5.8) numerically. The following system parameters were used:

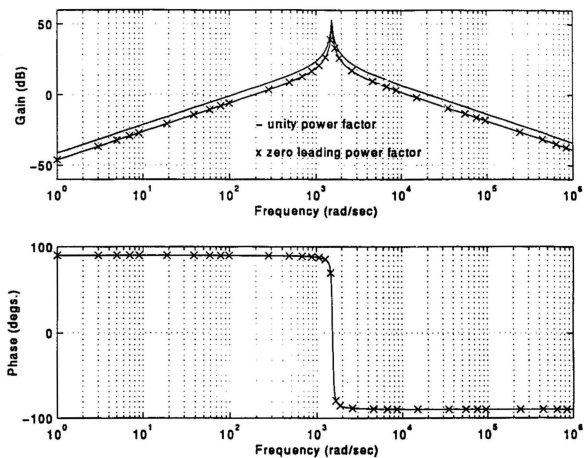


Figure 5.15: Bode plot of the open-loop transfer function of the inner current loop

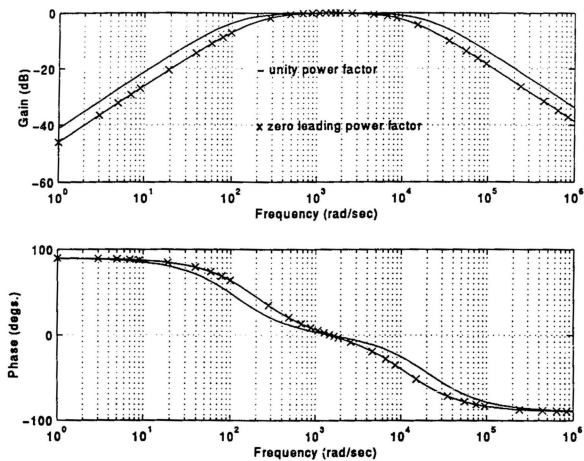


Figure 5.16: Bode plot of the closed-loop transfer function of the inner current loop for $k_{pc}=1.0$

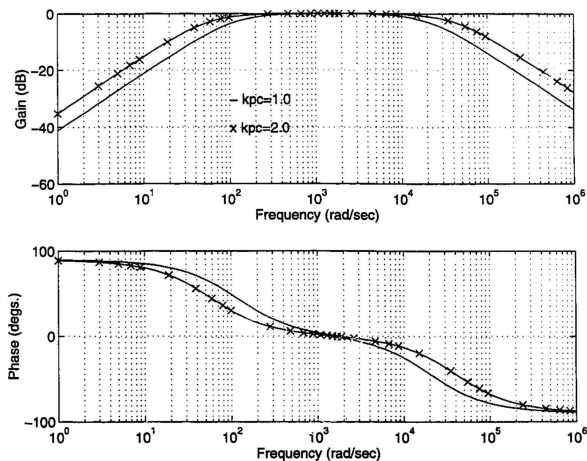


Figure 5.17: Effect of k_{pc} on the Bode plot of the closed-loop transfer function of the inner current loop for unity power factor operation

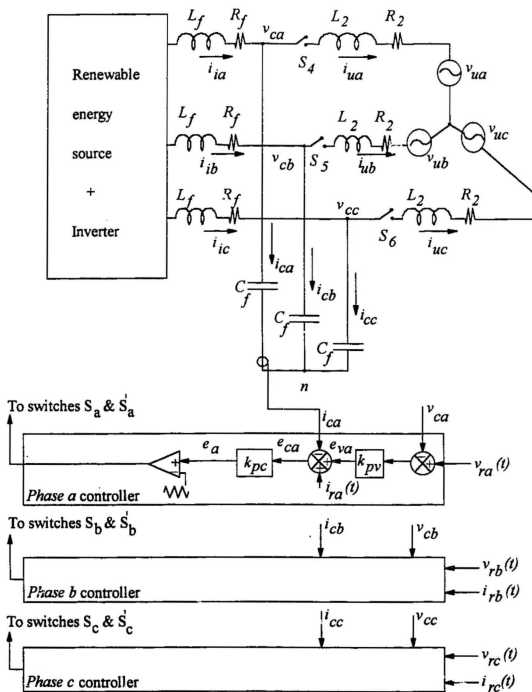


Figure 5.18: The closed-loop three-phase UIS

$$\begin{array}{lll}
L_s=10 \text{ mH}, & C_d=10\,000\mu\text{F} & L_f=L_2=5.0 \text{ mH}, \\
C_f=300.0 \mu\text{F}, & V_u=110.0 \text{ Volts (rms)}, & V_{dc}=300.0 \text{ Volts}, \\
I_u=7.07 \text{ Amp (rms)}, & k_{pc}=2.0, & k_{pu}=5.0.
\end{array}$$

The system is operated to feed the utility line current into the AC network at unity power factor.

Figure 5.19 shows the inverter output current of the three-phases. The figure shows that it takes about two cycles for the inverter output current to reach its steady-state balanced sinusoidal waveforms. The three-phase capacitor voltages are depicted in Fig. 5.20. The figure shows that the capacitor voltage faithfully follows its reference sinusoidal waveform with a small steady-state error.

Figure 5.21 shows the three-phase capacitor currents which are constrained by the control scheme to follow their respective reference waveforms with a small steady-state error. Figure 5.22 depicts the three-phase utility line currents. For the given circuit parameters, the expected utility line current is 20 Amperes peak-to-peak. It is observed from the figure that after approximately two cycles from “cold” start of the UIS, the utility line current reaches its steady-state value with very small steady-state error.

5.8 Summary

The characteristics of the three-phase UIS employing the proposed control scheme were presented. Low-frequency models in the θ - q - d rotating frame of reference were derived. Using the pole-zero map and the root-locus technique, the characteristics of the system for unity and zero-leading power factors were investigated. In particular, the effect of the two operating conditions on the stability of the system was presented. Computer simulation results of various waveforms in the UIS system at unity power

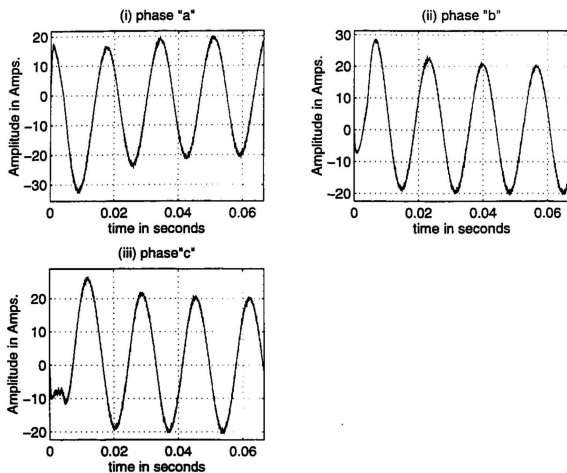


Figure 5.19: Computer simulation waveforms of the three-phase inverter output current: unity power factor operation

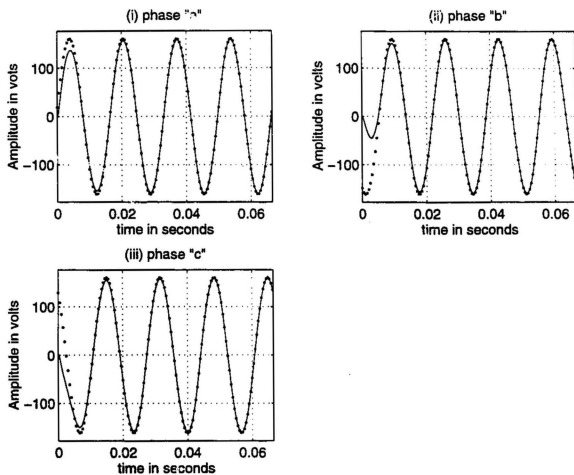


Figure 5.20: Computer simulation waveforms of the three-phase line-to-neutral capacitor (load) voltage: unity power factor operation

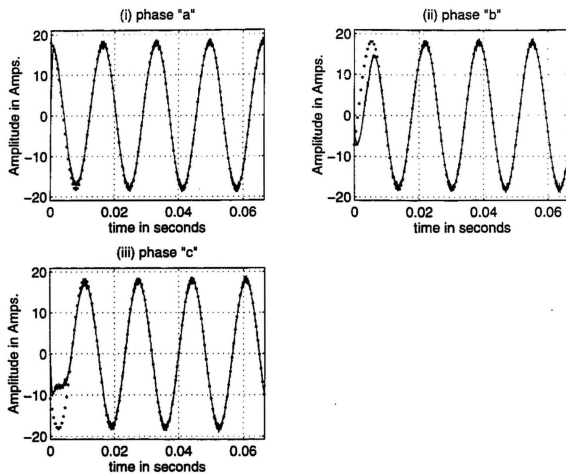


Figure 5.21: Computer simulation waveforms of the three-phase capacitor currents: unity power factor operation

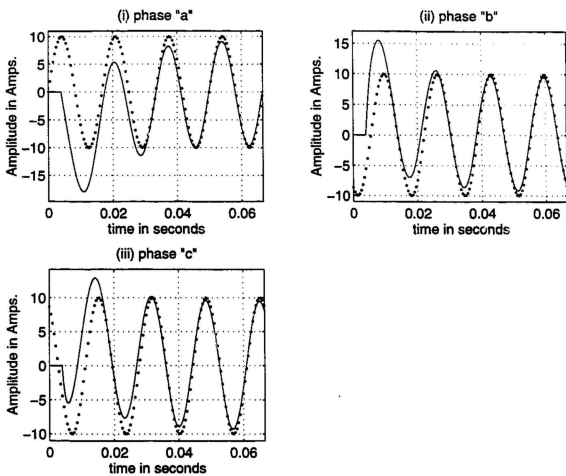


Figure 5.22: Computer waveforms simulation of the three-phase utility line current: unity power factor operation

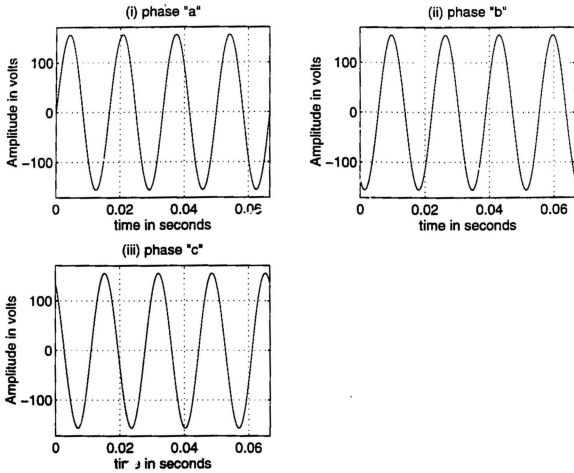


Figure 5.23: Computer simulation waveforms of the three-phase utility voltage

factor operation were presented. It was shown that the proposed control scheme results in stable operation of the three-phase voltage-source UIS for a wide range of variation in the operating modes.

Chapter 6

Summary and Conclusions

Static uninterruptible power supplies (UPS) and utility interactive systems (UIS) may employ the same power inverter topology, such as PWM inverter with an output filter. However, the control strategies for achieving the required output are very different. These variations are due to the fact that, in the UPS, the load voltage is controlled so that it follows a sinusoidal waveform, whereas, in the UIS, the utility line current is the variable to be controlled. To the best of the author's knowledge, there has been no attempt to develop a control scheme that can be applied to the two applications. In this study, a cost-effective and practical unified control scheme applicable to both voltage-source UPS and UIS was developed. The proposed scheme consists of a multiple feedback loop strategy with fixed switching frequency and variable duty cycle. The proposed controller is based on regulating the current in the capacitor of the load filter in an inner feedback loop while controlling the capacitor voltage in an outer feedback loop. In contrast to other feedback control schemes, such as the dead-beat and state-variable feedback techniques, this control strategy is insensitive to parameter variations, simple to implement, compact, and cost-effective. Moreover, this scheme lends itself to both linear and non-linear loads and weak AC networks

applications. Furthermore, it is capable of producing nearly perfect sinusoidal load voltage in the UPS and sinusoidal utility line current in the UIS with reasonable filter parameters and a moderate switching frequency.

The characteristics of the proposed controller for each of these systems was investigated as follows. At the outset, a single-phase UPS system was used as the vehicle to develop the proposed control scheme. A general model of the UPS system was first established and used to obtain simulation waveforms in the power inverter circuit. However, it was not possible to examine the system performance analytically due to the switching nature of the power inverter. Employing Fourier series analysis, the discrete system model was replaced by two time-continuous analytical models, namely, the low-frequency and the high-frequency models. The two models were used to establish a procedure for selecting optimum filter parameters of the UPS system.

The low-frequency model of the system was used to examine the system performance for frequencies lower than the inverter switching frequency. First, the non-linear analytical model was linearized using perturbation and small-signal approximations. Second, transfer functions describing the incremental dynamics of the power circuit state variables due to incremental changes in the control signal were derived from the linearized system model. It was shown that closing the control loop around the load (capacitor) voltage resulted in oscillatory behaviour of the UPS system. However, employing the capacitor current in an inner feedback loop and the capacitor voltage in an outer feedback loop resulted in stable and successful operation of the UPS system.

Employing Bode plots and time-domain error analysis, it was shown that proportional controllers in the feed-forward path of both the inner current and outer

voltage feedback loops were sufficient to produce a well-regulated and nearly perfect sinusoidal load voltage and excellent dynamic behaviour of the proposed UPS system. Experimental results of the proposed scheme for both linear and non-linear loads were provided to validate the predicted and simulation results.

The proposed scheme was extended to the three-phase UPS system with the DC input filter dynamics taken into account. To cope with the time-varying nature of the system matrix, the system state variables were transformed to a rotating frame of reference using the forward-backward transformation. The resultant system model was found to be non-linear but time-invariant.

A small-signal model was derived from the system low-frequency model in the rotating frame of reference using perturbations and small-signal approximation. The low-frequency model may be employed to derive various transfer functions of the three-phase UPS system. In this thesis, the transfer function of the incremental variation of the capacitor voltage, and current due to incremental changes in the modulating signal were derived and used to examine the incremental dynamics of the power circuit. It was shown that the proposed scheme results in stable operation of the three-phase UPS system. Computer simulation and experimental results were presented to show the feasibility of the proposed scheme and validate the analytical models of the three-phase UPS system.

In order to demonstrate its portability, the proposed control strategy was extended to the single-phase voltage-source UIS to shape and control the utility line current. First, it was shown that employing the utility line current as the only feedback variable in the control circuit results in unstable operation of the UIS system. However, employing the proposed control strategy (i.e. inner capacitor current and

outer capacitor voltage feedback loops) provided an indirect control of the utility line current. The scheme was capable of producing a nearly perfect sinusoidal utility line current at any desired phase angle with respect to the utility voltage. Thus, the proposed UIS can be employed as a static VAR compensator, or an active filter. It is also expected to be applicable to both weak and large AC network applications. Experimental results verifying the feasibility of the proposed control scheme with the utility line current injected at a phase angle of zero and 90° with respect to the utility voltage were reported in the thesis.

The modeling, analysis, and control procedures established for the three-phase UPS system were extended to three-phase UIS. However, in the latter case, the θ - q - d transformation was used because it decouples the active and reactive components of the power flow in the system. The characteristics of the system were examined for various modes of operation with regard to its stability. Computer simulation results showed that the system was capable of producing nearly perfect sinusoidal load voltage and utility line current, thus maintaining both voltage and current harmonics within the specifications for harmonic injection into the utility network.

Major contributions and achievements of the thesis in the area of UPS and UIS applications are summarized as follows.

1. Successful development of a simple and cost-effective control strategy that can be used in UPS as well as UIS applications.
2. General analytical models and analysis for each power supply application were developed. For the three-phase UIS, the θ - q - d transformation technique was used to obtain an equivalent circuit representation of the UIS. This circuit model can be used to provide additional insight into the behaviour of the system in a

similar manner to the equivalent circuit of AC motors.

3. Transfer functions relating the behaviour of incremental variations of the state variables of the power circuit to incremental changes in the control circuit were derived. The transfer functions, along with the corresponding pole-zero map provided insight into the effect of system parameters on the dynamic behaviour of the systems. Detailed characteristics of both UPS and UIS were provided.
4. Systematic procedures for choosing filter parameters of the power circuit, and appropriate feedback variables and feed-forward controllers in the control circuit were established in order to achieve stable and successful operation of the feedback control of the power circuit.
5. Laboratory implementation of the voltage-source single-phase half-bridge and three-phase full-bridge inverter configuration for UPS systems and the single-phase UIS. The systems included analog/digital implementation of the proposed control scheme, and a soft-start circuit to bring both the UPS systems and UIS from “cold” start to full-load with no in-rush current in the power circuit during the transient stage of the power circuit.

6.1 Suggestions for Future Work

The present work focused on the development of a control strategy for UPS systems and UIS. To this end, the thesis provided modelling and analysis of the UPS and UIS systems which incorporate the proposed multiple feedback loop control scheme. Experimental verification of the single-phase UPS and UIS, and the three-phase UPS system have demonstrated the feasibility of the proposed scheme. Efforts are under

way to implement the three-phase UIS. However, further work needs to be carried out to improve the performance of the proposed controller in the UPS and UIS applications.

- Dead-time intervals in PWM inverters result in low utilization of the inverter input voltage and generation of low-order harmonics in the inverter output voltage. For renewable energy source, poor voltage utilization reduces the power extracted from the renewable energy source. Several dead-time compensation techniques have been proposed in the literature [108]-[110]. Further work needs to be carried out to develop a compensator to be incorporated in the proposed control scheme to compensate for the loss of the inverter output voltage.
- In this study, only proportional controllers were used in the feedback loops. Although it was shown that good dynamic and steady-state performances were achieved, the use of proportional-plus-integral (PI) controller in the outer voltage loop is expected to reduce the steady-state error. However, implementing the PI controller in the stationary frame of reference where the controlled quantities are AC introduces phase errors. Implementation of the PI regulator in the rotating frame of reference is expected to overcome this problem and thus needs to be examined.
- Although the general models of the three-phase systems are applicable to unbalanced load, subsequent analysis concentrated on balanced load operation. Unbalanced operation is likely to have adverse effect on the operation of the system. Further work is required to examine the performance of the system under these conditions.

- The system is capable of feeding the line current at zero-leading and unity power factors with respect to the utility voltage with very fast dynamic response and high quality of line current. The fast dynamic performance of the control scheme is expected to cope well with weak AC networks where both voltage and frequency fluctuations can be simultaneously present. The system is also expected to significantly reduce voltage harmonics imposed on neighbouring customers by conventional UIS circuits. Further work is required to test the UIS in the presence of a weak AC network.

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Appendix A

Control Circuit of the Proposed Control Scheme

In order to verify the performance of the proposed scheme, laboratory models of the single-phase and three-phase UPS and the single-phase UIS were constructed. Figure A.1 shows the circuit diagram of the proposed single-phase UPS system. A soft-start mechanism was employed to bring the system from “cold” start to full-load. At first, the outer voltage loop gain was set to zero and was gradually increased to its full-load designed value after one complete cycle. This mechanism has the effect of significantly reducing the starting current in the filter capacitor and controlling the in-rush current. The details of the soft-start circuit are given in Fig. A.2.

Figure A.3 shows the block diagram for generating the high-frequency carrier waveform. The waveform is generated by using a phase-locked loop (PLL) circuit as a frequency multiplier. This is achieved by passing the reference signal through a zero-crossing detector to create a square waveform from the sinusoidal reference waveform. This square waveform becomes the input to the PLL circuit. A frequency counter was inserted in the feedback loop of the PLL circuit such that the output triangular waveform is in synchronism with its frequency set as a multiple integer of

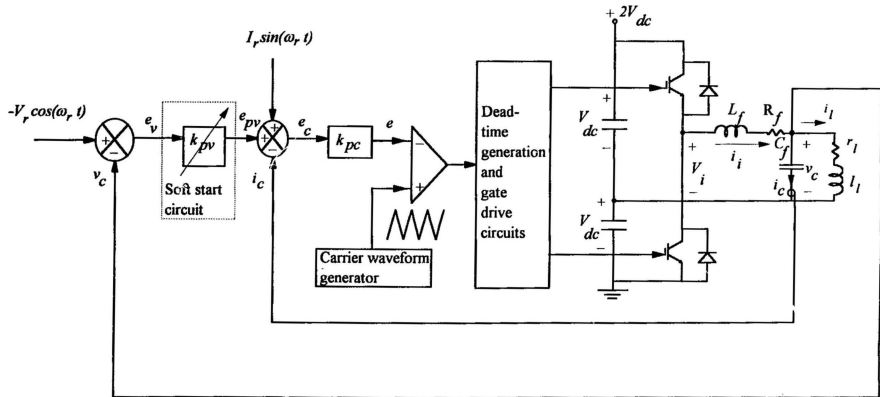


Figure A.1: Circuit diagram of the proposed control strategy for the single phase UPS system

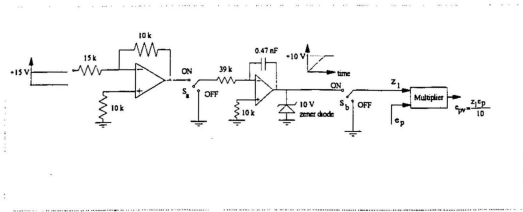


Figure A.2: Soft-start circuit

the reference frequency.

Since inverter power switching devices require finite time to turn ON/OFF, a look-out circuit was employed to generate a dead-time interval when switching from an upper to a lower switching device or vice versa in the same inverter leg. The block and timing diagrams for generating this dead-time interval are shown in i gs. A.4 and A.5 respectively. Figure A.6 shows a photograph of the experimental setup of the three-phase UPS system employing the proposed control strategy. Figures A.7 and A.8 show close-up views of the power and control circuits respectively.

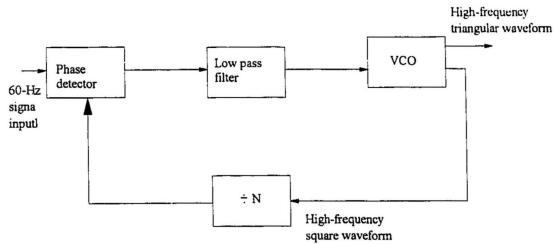


Figure A.3: Block diagram of the carrier waveform generation

Figure A.4: Block diagram of the logic circuit for dead-time generation

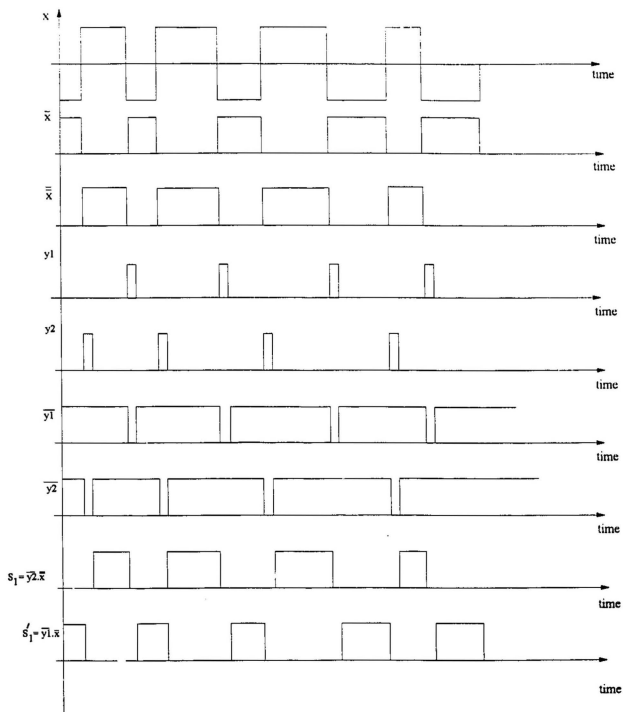


Figure A.5: Timing diagram for dead-time generation

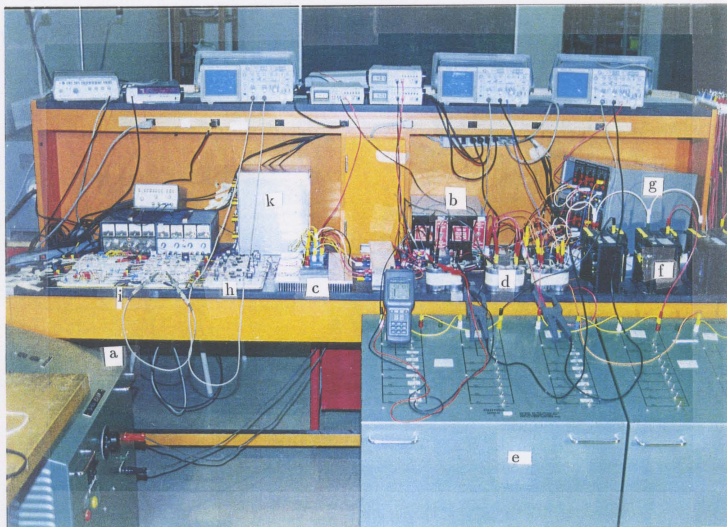


Figure A.6: Photograph of the prototype three-phase UPS system : (a) DC power supply, (b) input DC capacitor, (c) three-phase bridge inverter, (d) load filter capacitor, (e) load resistance, (f) load inductor, (g) voltage and current sensors, (h) gate-drive circuit of the power transistors, (i) control circuit, (k) power supply for the gate drive circuit

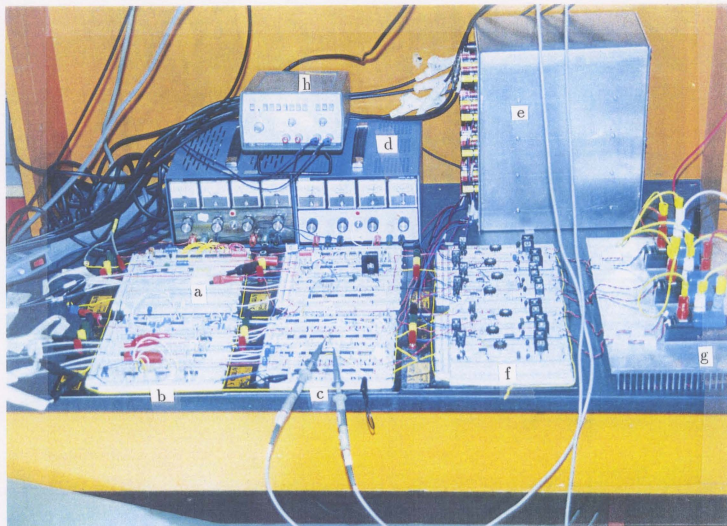


Figure A.7: Photograph of the control circuit of the prototype three-phase UPS system: (a) carrier waveform generator, (b) three-phase reference waveform generation, and current and voltage filters, (c) electronic circuit of the proposed controller, (d) power supply of the control circuit, (e) power supply of the gate-drive circuit of the power transistors, (f) gate-drive circuit of the power transistors, (g) three-phase bridge inverter

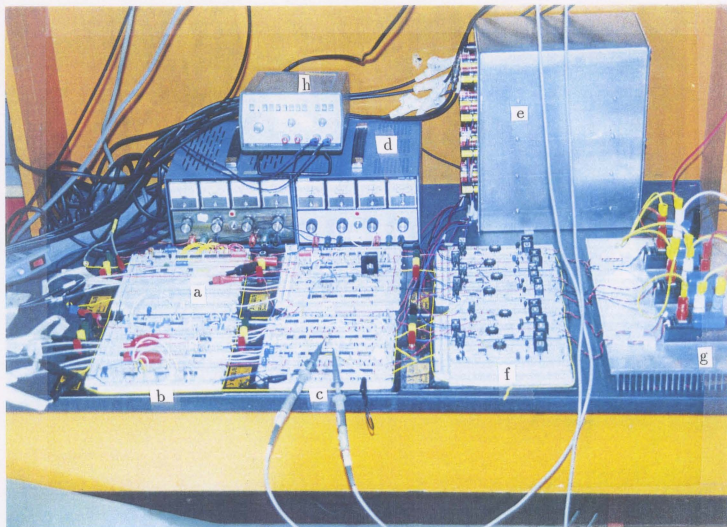


Figure A. 7: Photograph of the control circuit of the prototype three-phase UPS system: (a) carrier waveform generator, (b) three-phase reference waveform generation, and current and voltage filters, (c) electronic circuit of the proposed controller, (d) power supply of the control circuit, (e) power supply of the gate-drive circuit of the power transistors, (f) gate-drive circuit of the power transistors, (g) three-phase bridge inverter

